



TSA0801

8-BIT, 40MSPS, 40mW A/D CONVERTER

- 8-bit A/D converter in deep submicron CMOS technology
- Single supply voltage: 2.5V
- Input range: 2Vpp differential
- 40MSPS sampling frequency
- Ultra low power consumption: 40mW @ 40MHz (10mW @ 5MSPS)
- ENOB=7.9 @ Nyquist
- SFDR typically up to 67dB @ Fs=40MSPS, Fin=5MHz
- Built-in reference voltage with external bias capability
- STMicroelectronics 8, 10, 12 and 14-bits ADC pinout compatibility

DESCRIPTION

The TSA0801 is an 8-bit, 40MHz sampling frequency Analog to Digital converter using a deep submicron CMOS technology combining high performances and very low power consumption.

The TSA0801 is based on a pipeline structure and digital error correction to provide excellent static linearity and go beyond 7.9 effective bits at Fs=40MSPS, and Fin=10MHz.

A voltage reference is integrated in the circuit to simplify the design and minimize external components. It is nevertheless possible to use the circuit with an external reference.

Differential or single-ended analog inputs can be applied to the converter. A tri-state capability is available on the outputs. The output data can be coded into two different formats. A Data Ready signal is raised as the data is valid on the output and can be used for synchronization purposes.

The TSA0801 is available in commercial (0 to +70°C) and extended (-40 to +85°C) temperature range, in a small 48 pins TQFP package.

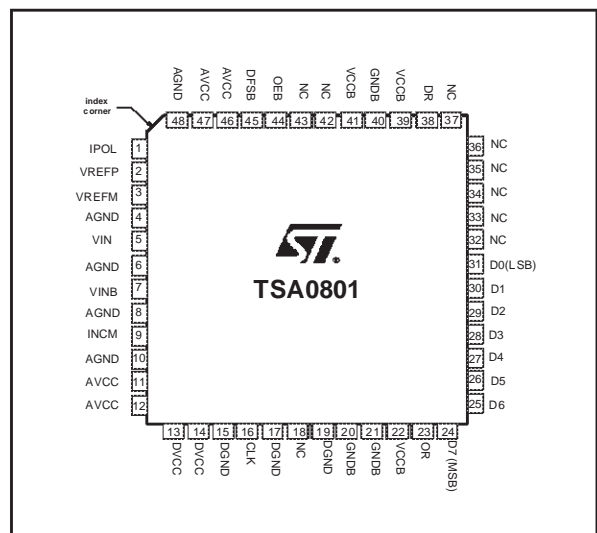
APPLICATIONS

- Hand-held instrumentation
- Camcorders
- Computer scanners
- Digital communication

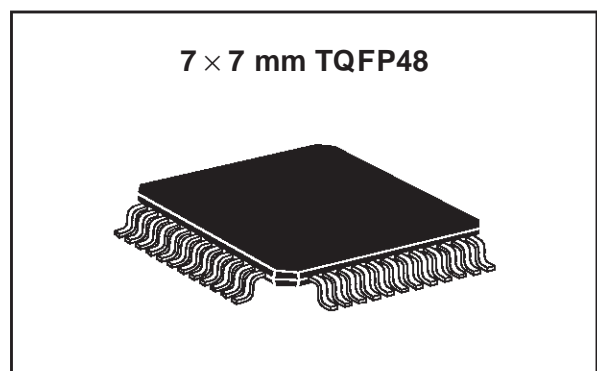
ORDER CODE

Part Number	Temperature Range	Package	Conditioning	Marking
TSA0801CF	0°C to +70°C	TQFP48	Tray	SA0801C
TSA0801CFT	0°C to +70°C	TQFP48	Tape & Reel	SA0801C
TSA0801IF	-40°C to +85°C	TQFP48	Tray	SA0801I
TSA0801IFT	-40°C to +85°C	TQFP48	Tape & Reel	SA0801I
EVAL0801/AA	Evaluation board			

PIN CONNECTIONS (top view)



PACKAGE



TSA0801

ABSOLUTE MAXIMUM RATINGS

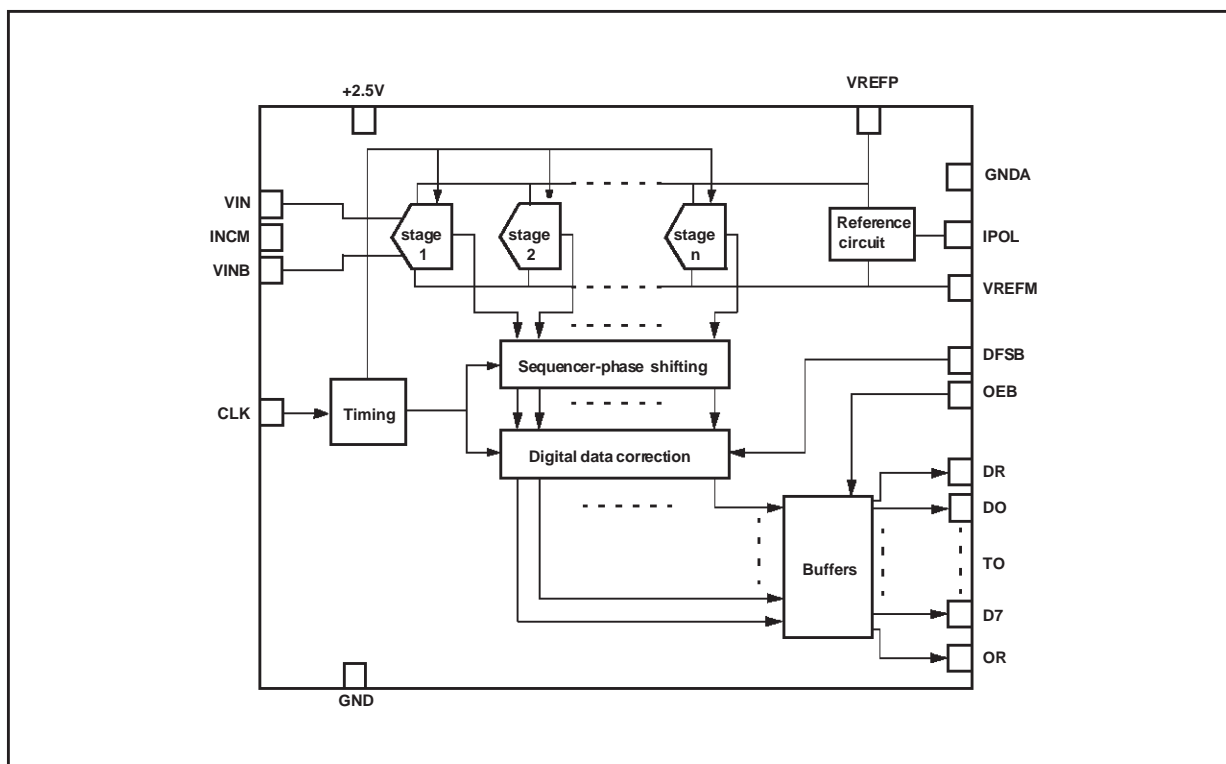
Symbol	Parameter	Values	Unit
AVCC	Analog Supply voltage ¹⁾	0 to 3.3	V
DVCC	Digital Supply voltage ¹⁾	0 to 3.3	V
VCCB	Digital buffer Supply voltage ¹⁾	0 to 3.3	V
IDout	Digital output current	-100 to 100	mA
Tstg	Storage temperature	+150	°C
ESD	Electrical Static Discharge:		
	- HBM - CDM-JEDEC Standard	2 1.5	KV

1) All voltages values, except differential voltage, are with respect to network ground terminal. The magnitude of input and output voltages must never exceed -0.3V or VCC+0V

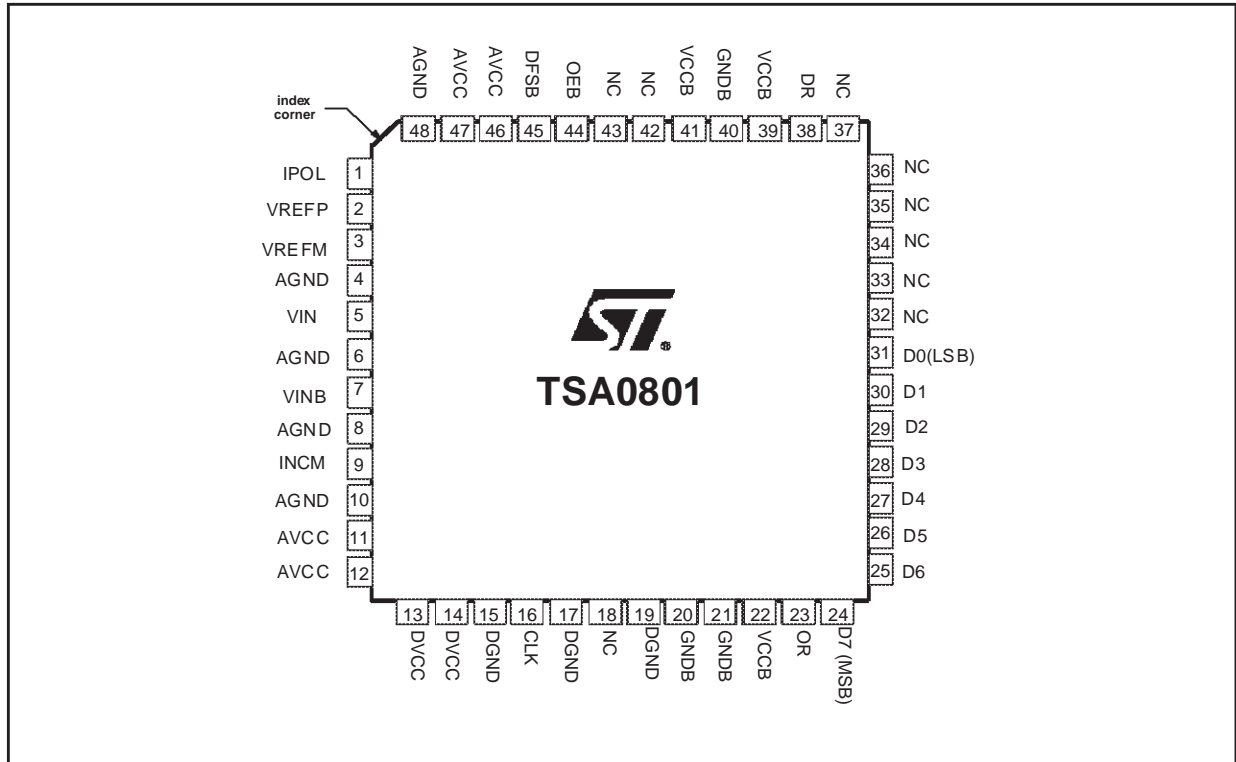
OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AVCC	Analog Supply voltage		2.25	2.5	2.7	V
DVCC	Digital Supply voltage		2.25	2.5	2.7	V
VCCB	Digital buffer Supply voltage		2.25	2.5	2.7	V
VREFP	Forced top voltage reference		1.16	-	AVCC	V
VREFM	Forced bottom reference voltage		0	0	0.5	V

BLOCK DIAGRAM



PIN CONNECTIONS (top view)



PIN DESCRIPTION

Pin No	Name	Description	Observation	Pin No	Name	Description	Observation
1	IPOL	Analog bias current input		25	D6	Digital output	CMOS output (2.5V)
2	VREFP	Top voltage reference	1V	26	D5	Digital output	CMOS output (2.5V)
3	VREFM	Bottom voltage reference	0V	27	D4	Digital output	CMOS output (2.5V)
4	AGND	Analog ground	0V	28	D3	Digital output	CMOS output (2.5V)
5	VIN	Analog input	1Vpp	29	D2	Digital output	CMOS output (2.5V)
6	AGND	Analog ground	0V	30	D1	Digital output	CMOS output (2.5V)
7	VINB	Inverted analog input	1Vpp	31	D0(LSB)	Digital output	CMOS output (2.5V)
8	AGND	Analog ground	0V	32	NC	Non connected	
9	INCM	Input common mode	0.5V	33	NC	Non connected	
10	AGND	Analog ground	0V	34	NC	Non connected	
11	AVCC	Analog power supply	2.5V	35	NC	Non connected	
12	AVCC	Analog power supply	2.5V	36	NC	Non connected	
13	DVCC	Digital power supply	2.5V	37	NC	Non connected	
14	DVCC	Digital power supply	2.5V	38	DR	Data Ready output	CMOS output (2.5V)
15	DGND	Digital ground	0V	39	VCCB	Digital Buffer power supply	2.5V
16	CLK	Clock input	2.5V compatible CMOS input	40	GNDB	Digital Buffer ground	0V
17	DGND	Digital ground	0V	41	VCCB	Digital Buffer power supply	2.5V
18	NC	Non connected		42	NC	Non connected	
19	DGND	Digital ground	0V	43	NC	Non connected	
20	GNDB	Digital buffer ground	0V	44	OEB	Output Enable input	2.5V compatible CMOS input
21	GNDB	Digital buffer ground	0V	45	DFSB	Data Format Select input	2.5V compatible CMOS input
22	VCCB	Digital buffer power supply	2.5V	46	AVCC	Analog power supply	2.5V
23	OR	Out Of Range output	CMOS output (2.5V)	47	AVCC	Analog power supply	2.5V
24	D7(MSB)	Most Significant Bit output	CMOS output (2.5V)	48	AGND	Analog ground	0V

TSA0801

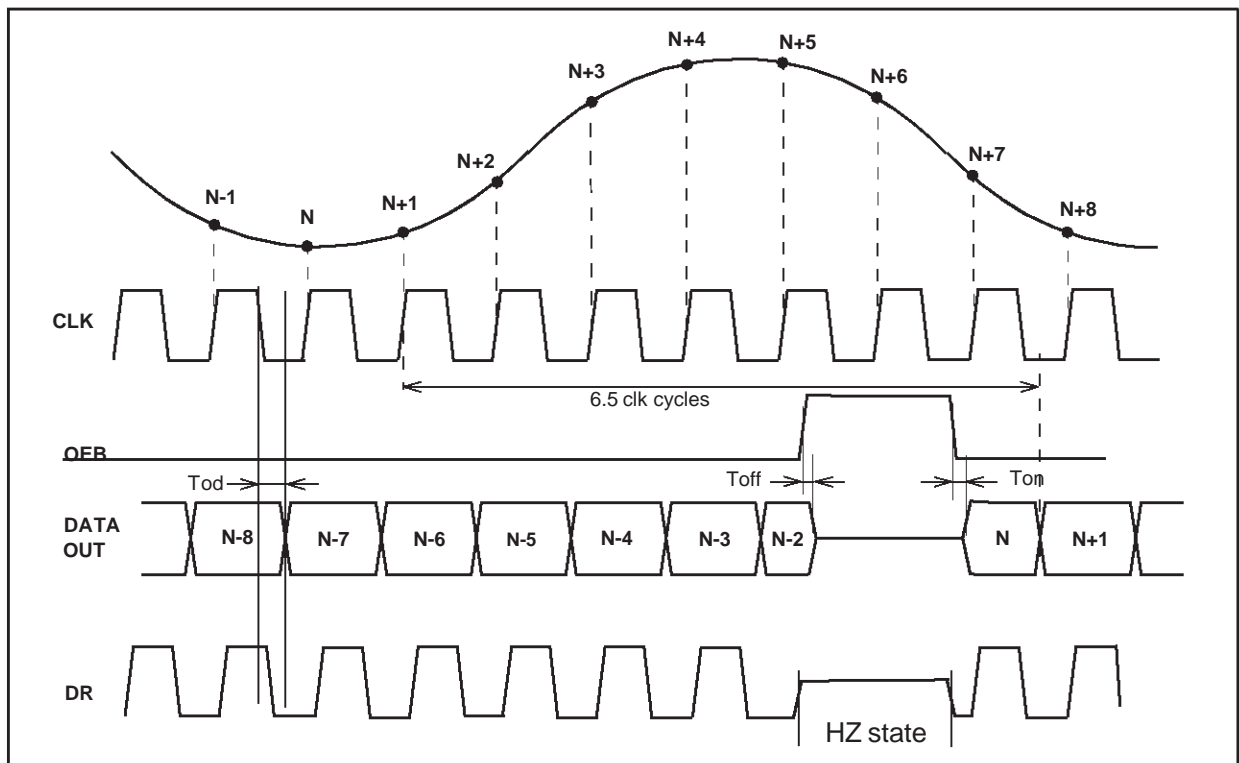
ELECTRICAL CHARACTERISTICS

AVCC = DVCC = VCCB = 2.5V, Fs= 40MSPS, Fin=1MHz, Vin@ -1.0dBFS, VREFM = 0V
 Tamb = 25°C (unless otherwise specified)

TIMING CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
FS	Sampling Frequency		0.5		40	MHz
DC	Clock Duty Cycle		45	50	55	%
TC1	Clock pulse width (high)		11	12.5		ns
TC2	Clock pulse width (low)		11	12.5		ns
Tod	Data Output Delay (Fall of Clock to Data Valid)	10pF load capacitance		5		ns
Tpd	Data Pipeline delay			6.5		cycles
Ton	Falling edge of OEB to digital output valid data			1		ns
Toff	Rising edge of OEB to digital output tri-state			1		ns

TIMING DIAGRAM



CONDITIONS

AVCC = DVCC = VCCB = 2.5V, Fs= 40Msps, Fin= 1MHz, Vin@ -1.0dBFS, VREFM= 0V
 Tamb = 25°C (unless otherwise specified)

ANALOG INPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VIN-VINB	Full scale reference voltage			2.0		Vpp
Cin	Input capacitance			7.0		pF
BW	Analog Input Bandwidth	Vin@ -1dBFS, FS=40Msps		100		MHz
ERB	Effective Resolution Bandwidth ¹⁾			60		MHz

1) See parameters definition for more information

REFERENCE VOLTAGE

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VREFP	Top internal reference voltage		0.89	1.03	1.16	V
		Tmin= -40°C to Tmax= 85°C ¹⁾	0.88		1.16	V
Vpol	Analog bias voltage		1.19	1.27	1.35	V
		Tmin= -40°C to Tmax= 85°C ¹⁾	1.18		1.36	V
Ipol	Analog bias current	Normal operating mode	50	70	100	μA
Ipol	Analog bias current	Shutdown mode		0		μA
VINCM	Input common mode voltage		0.46	0.57	0.66	V
		Tmin= -40°C to Tmax= 85°C ¹⁾	0.46		0.66	V

1) Not fully tested over the temperature range. Guaranteed by sampling.

TSA0801

CONDITIONS

AVCC = DVCC = VCCB = 2.5V, Fs= 40Msps, Fin= 1MHz, Vin@ -1.0dBFS, VREFP=1V, VREFM= 0V
Tamb = 25°C (unless otherwise specified)

POWER CONSUMPTION

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ICCA	Analog Supply current	1)		15.8	20	mA
		Tmin= -40°C to Tmax= 85°C ²⁾			21	mA
ICCD	Digital Supply Current	1)		1.3	2	mA
		Tmin= -40°C to Tmax= 85°C ²⁾			2	mA
ICCB	Digital Buffer Supply Current	1)		2.1	5	mA
		Tmin= -40°C to Tmax= 85°C ²⁾			5	mA
ICCBZ	Digital Buffer Supply Current in High Impedance Mode	1)		50	110	μA
Pd	Power consumption in normal operation mode	1)		48	60	mW
		Tmin= -40°C to Tmax= 85°C ²⁾			62	mW
PdZ	Power consumption in High Impedance mode	1)		43	55	mW
Rthja	Junction-ambient thermal resistor (TQFP48)			80		°C/W
Rthjc	Junction-case thermal resistor (TQFP48)			18		°C/W

1) Rpol= 18KΩ. Equivalent load: Rload= 470Ω and Cload= 6pF

2) Not fully tested over the temperature range. Guaranteed by sampling.

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Digital inputs						
VIL	Logic "0" voltage				0.8	V
VIH	Logic "1" voltage		2.0			V
Digital Outputs						
VOL	Logic "0" voltage	Iol=10μA			0.4	V
VOH	Logic "1" voltage	Ioh=10μA	2.4			V
IOZ	High Impedance leakage current	OEB set to VIH	-1.5		1.5	μA
CL	Output Load Capacitance				15	pF

ACCURACY

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
OE	Offset Error					mV
DNL	Differential Non Linearity		-0.5		+0.5	LSB
INL	Integral Non Linearity		-1		+1	LSB
-	Monotonicity and no missing codes		Guaranted			

CONDITIONS

AVCC = DVCC = 2.5V, Fs= 40Msps, Vin@ -1.0dBFS, VREFP=1V, VREFM= 0V

Tamb = 25°C (unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SFDR	Spurious Free Dynamic Range	Fin= 5MHz	60	68		dBc
		Fin= 10MHz 1)	60	68		
		Fin= 24MHz	60	67.7		
		Fin= 5MHz	60			dBc
Fin= 10MHz 2)	60					
Fin= 24MHz	59.8					
SNR	Signal to Noise Ratio	Fin= 5MHz	48	48.8		dB
		Fin= 10MHz 1)	48	48.8		
		Fin= 24MHz	48	48.8		
		Fin= 5MHz	48			dB
Fin= 10MHz 2)	48					
Fin= 24MHz	48					
THD	Total Harmonic Distortion	Fin= 5MHz	56	72.5		dB
		Fin= 10MHz 1)	56	72.5		
		Fin= 24MHz	56	67		
		Fin= 5MHz	57			dB
Fin= 10MHz 2)	55					
Fin= 24MHz	57					
SINAD	Signal to Noise and Distortion-Ratio	Fin= 5MHz	48	48.7		dB
		Fin= 10MHz 1)	48	48.7		
		Fin= 24MHz	48	48.7		
		Fin= 5MHz	48			dB
Fin= 10MHz 2)	48					
Fin= 24MHz	48					
ENOB	Effective Number of Bits	Fin= 5MHz	7.8	7.97		bits
		Fin= 10MHz 1)	7.8	7.97		
		Fin= 24MHz	7.8	7.96		
		Fin= 5MHz	7.8			bits
Fin= 10MHz 2)	7.8					
Fin= 24MHz	7.8					

1) Rpol= 18KΩ. Equivalent load: Rload= 470Ω and Cload= 6pF

2) Tmin= -40°C to Tmax= 85°C. Not fully tested over the temperature range. Guaranteed by sampling.

DEFINITIONS OF SPECIFIED PARAMETERS**STATIC PARAMETERS**

Static measurements are performed through method of histograms on a 2MHz input signal, sampled at 40MSPs, which is high enough to fully characterize the test frequency response. The input level is +1dBFS to saturate the signal.

Differential Non Linearity (DNL)

The average deviation of any output code width from the ideal code width of 1LSB.

Integral Non linearity (INL)

An ideal converter presents a transfer function as being the straight line from the starting code to the ending code. The INL is the deviation for each transition from this ideal curve.

DYNAMIC PARAMETERS

Dynamic measurements are performed by spectral analysis, applied to an input sinewave of various frequencies and sampled at 40MSPs.

Spurious Free Dynamic Range (SFDR)

The ratio between the amplitude of fundamental tone (signal power) and the power of the worst spurious signal (not always an harmonic) over the full Nyquist band. It is expressed in dBc.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to Noise Ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_s/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to Noise and Distorsion Ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). It is expressed in dB.

From the SINAD, the Effective Number of Bits (ENOB) can easily be deduced using the formula: $SINAD = 6.02 \times ENOB + 1.76$ dB.

When the applied signal is not Full Scale (FS), but has an A_0 amplitude, the SINAD expression becomes:

$SINAD = 6.02 \times ENOB + 1.76$ dB + $20 \log(2A_0/FS)$
The ENOB is expressed in bits.

Analog Input Bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3dB. Higher values can be achieved with smaller input levels.

Effective Resolution Bandwidth (ERB)

The band of input signal frequencies that the ADC is intended to convert without losing linearity i.e. the maximum analog input frequency at which the SINAD is decreased by 3dB or the ENOB by 1/2 bit.

Pipeline delay

Delay between time when the analog input is initially sampled and time when the corresponding digital data output is valid on the output bus. Also called data latency. It is expressed as a number of clock cycles.

EQUIVALENT CIRCUITS

Figure 1 : Analog Input Circuit

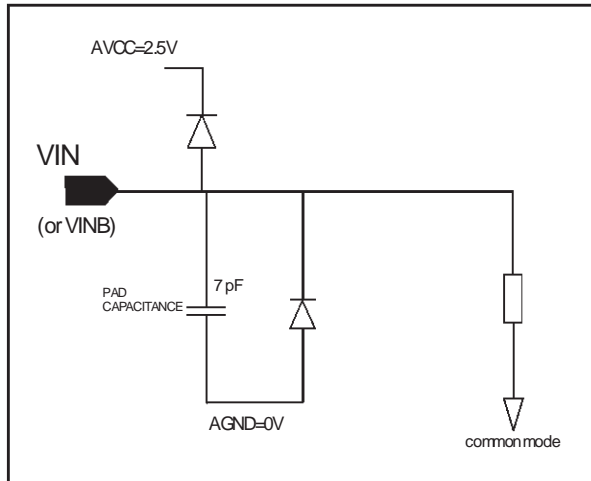


Figure 3 : Input buffers

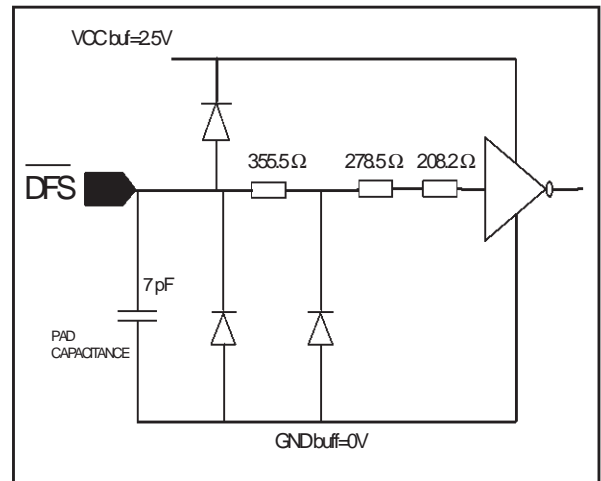


Figure 2 : Input clock circuit

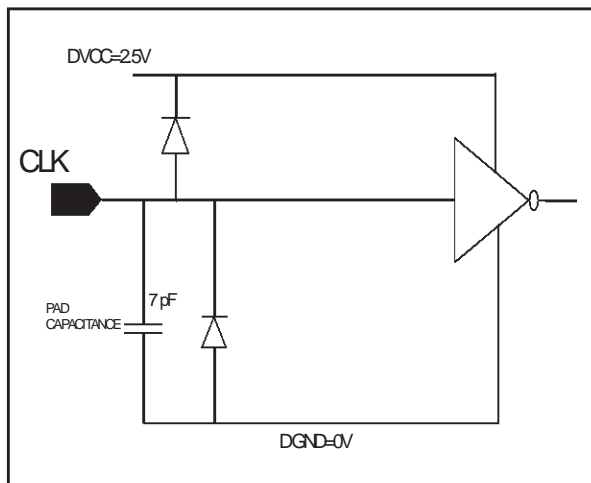
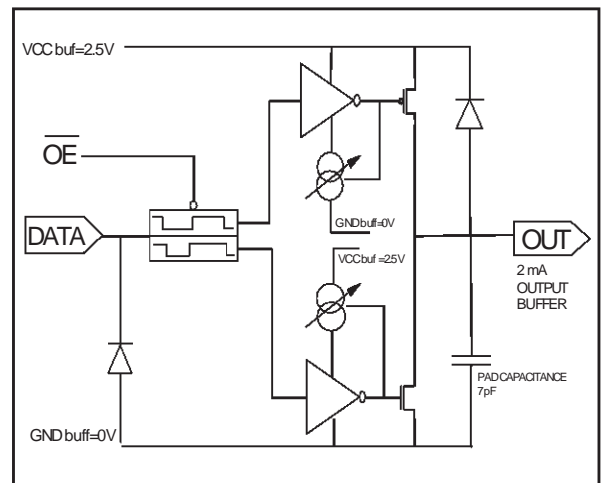


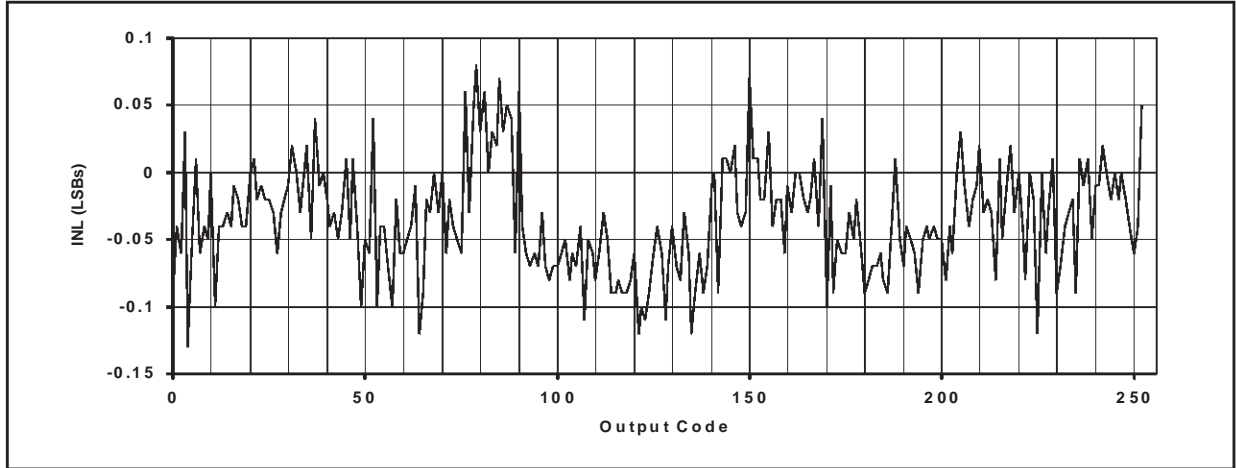
Figure 4 : Tri-state output buffers



TSA0801

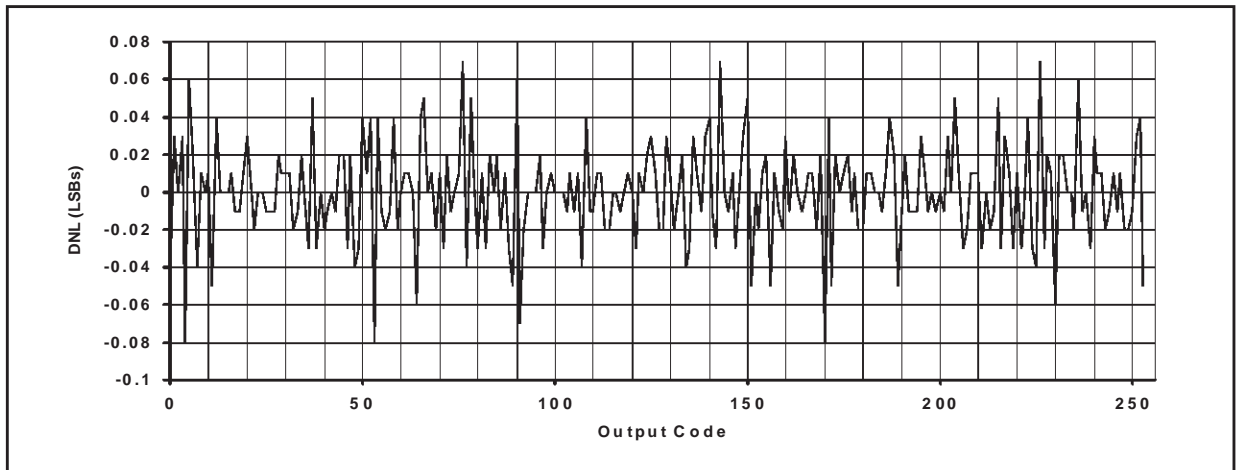
Static parameter: Integral Non Linearity

$F_s=40\text{MSPS}$; $F_{in}=1\text{MHz}$; $I_{cca}=11\text{mA}$; $N=65536\text{pts}$



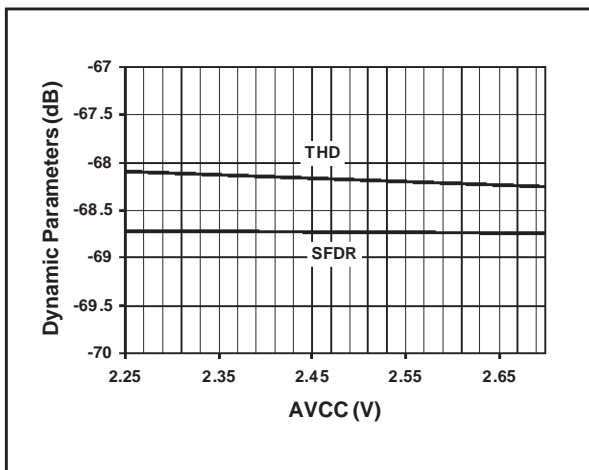
Static parameter: Differential Non Linearity

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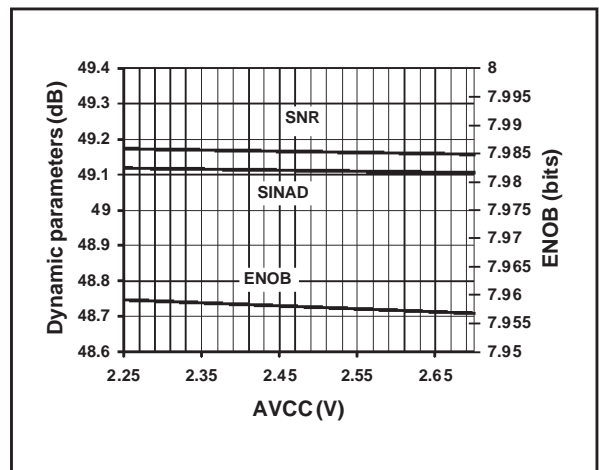
Linearity vs. AVcc

$F_s=40\text{MSPS}$; $I_{cca}=11\text{mA}$; $F_{in}=1\text{MHz}$



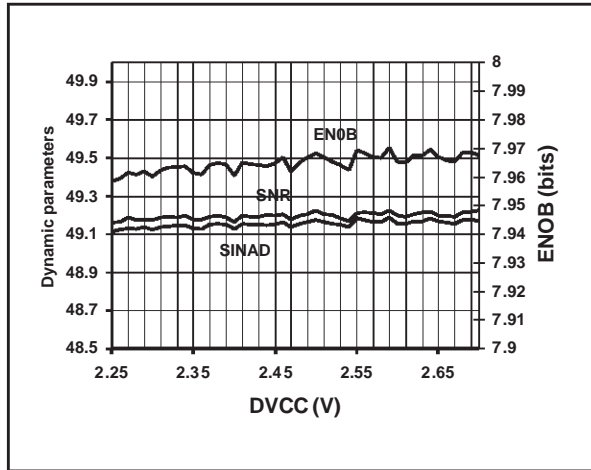
Distortion vs. AVcc

$F_s=40\text{MSPS}$; $I_{cca}=11\text{mA}$; $F_{in}=1\text{MHz}$



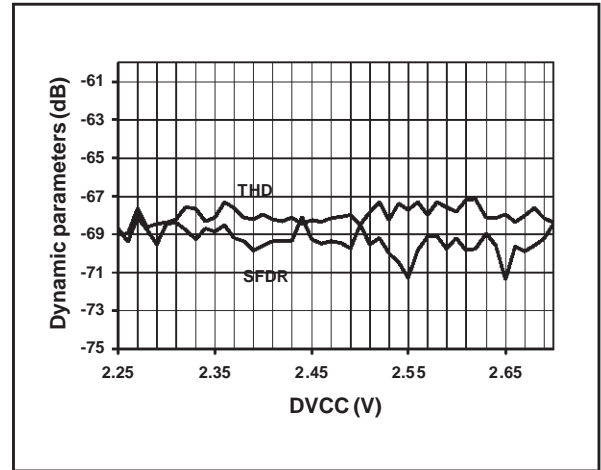
Linearity vs. DVcc

Fs=40MSPS; Icca=11mA; Fin=1MHz



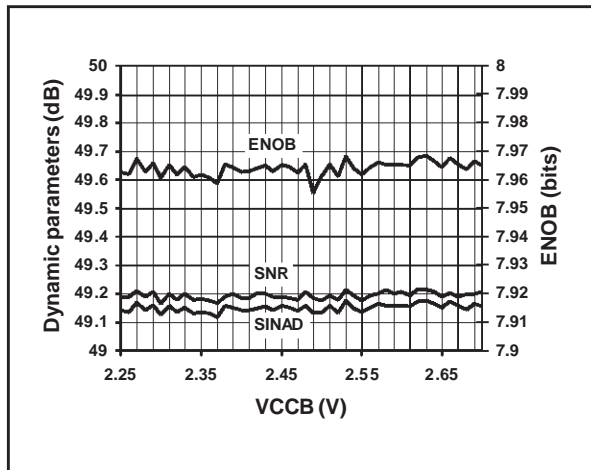
Distortion vs. DVcc

Fs=40MSPS; Icca=11mA; Fin=1MHz



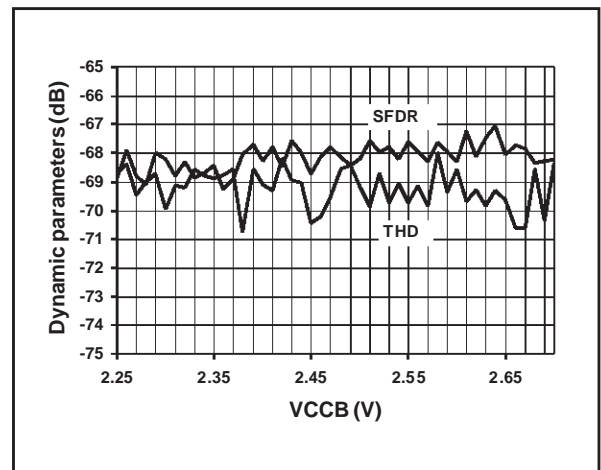
Linearity vs. Vccb

Fs=40MSPS; Icca=11mA; Fin=1MHz



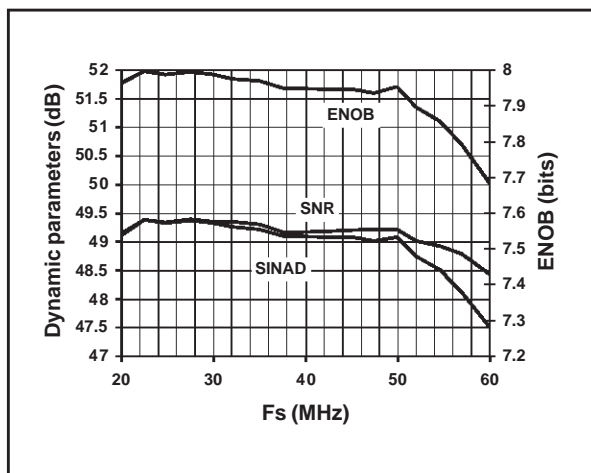
Distortion vs. Vccb

Fs=40MSPS; Icca=11mA; Fin=1MHz



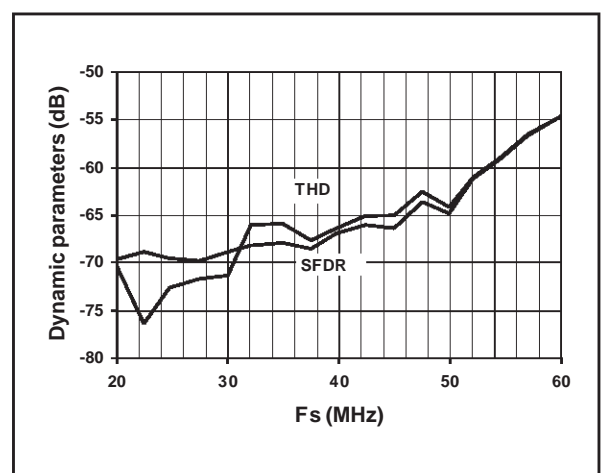
Linearity vs. Fs

Icca=11mA; Fin=5MHz



Distortion vs. Fs

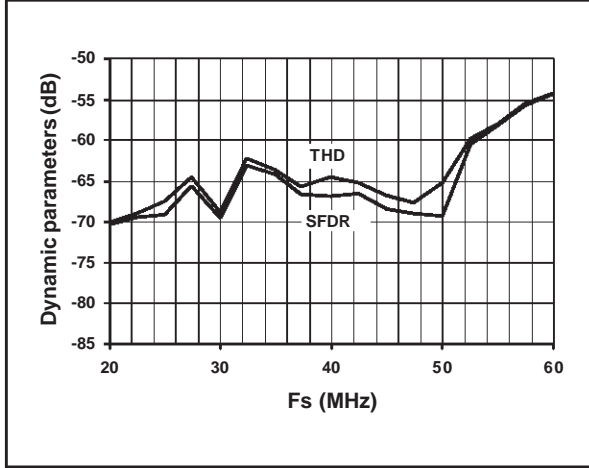
Icca=11mA; Fin=5MHz



TSA0801

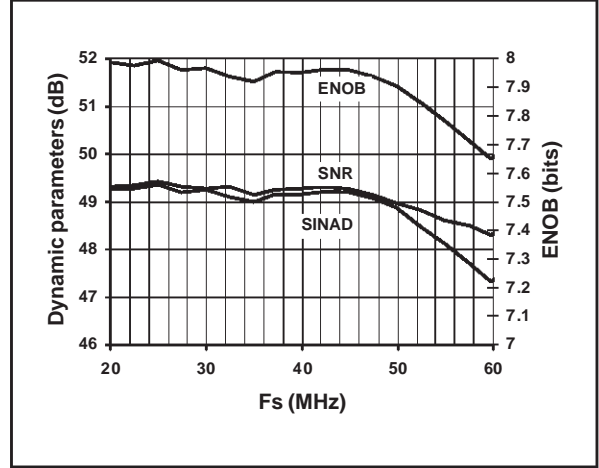
Linearity vs. Fs

Icca=11mA; Fin=15MHz



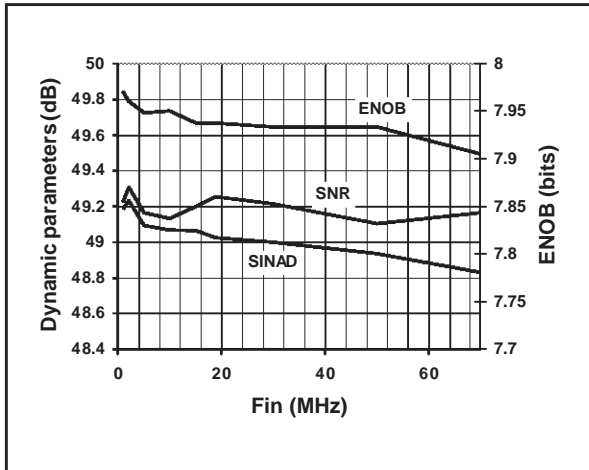
Distortion vs. Fs

Icca=11mA; Fin=15MHz



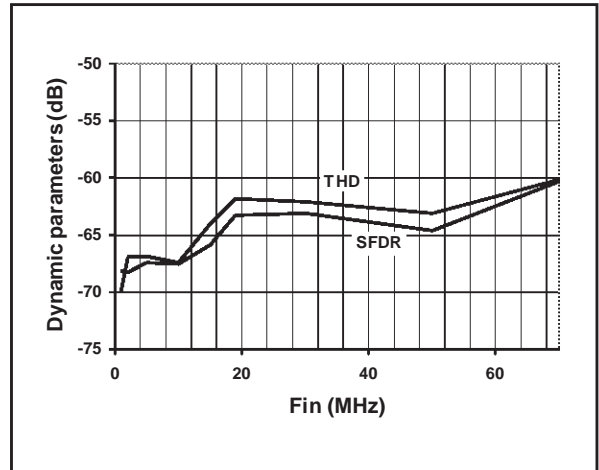
Linearity vs. Fin

Fs=40MSPS; Icca=11mA



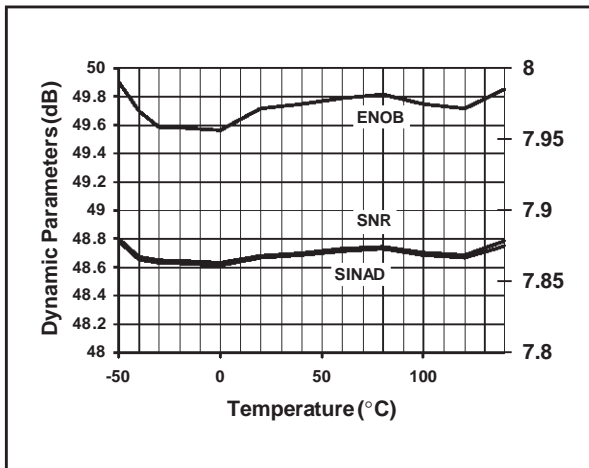
Distortion vs. Fin

Fs=40MSPS; Icca=11mA



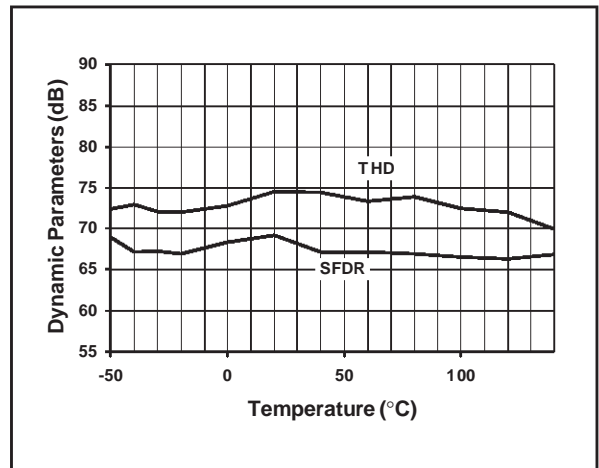
Linearity vs. Temperature

Fs=40MSPS; Icca=11mA; Fin=5MHz



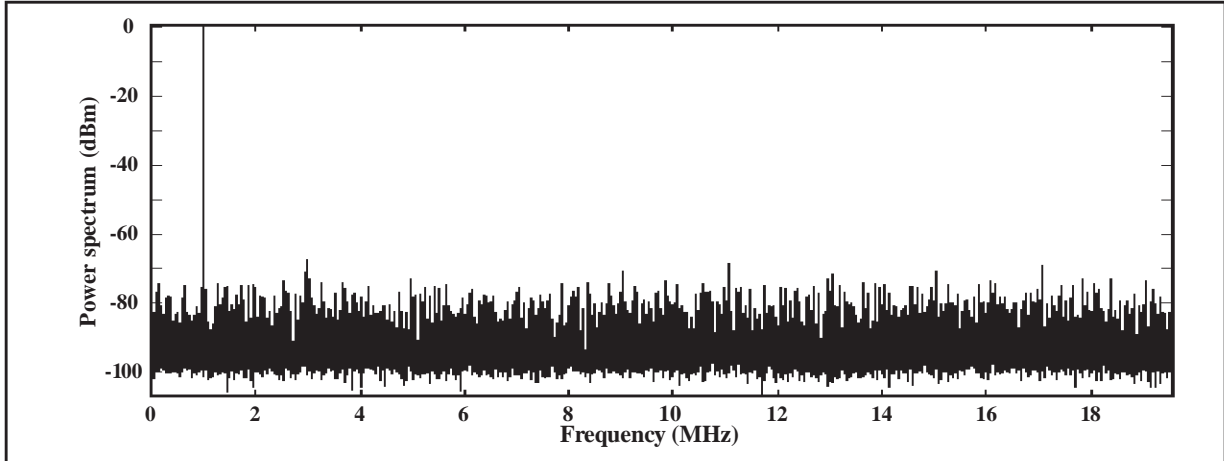
Distortion vs. Temperature

Fs=40MSPS; Icca=11mA; Fin=5MHz

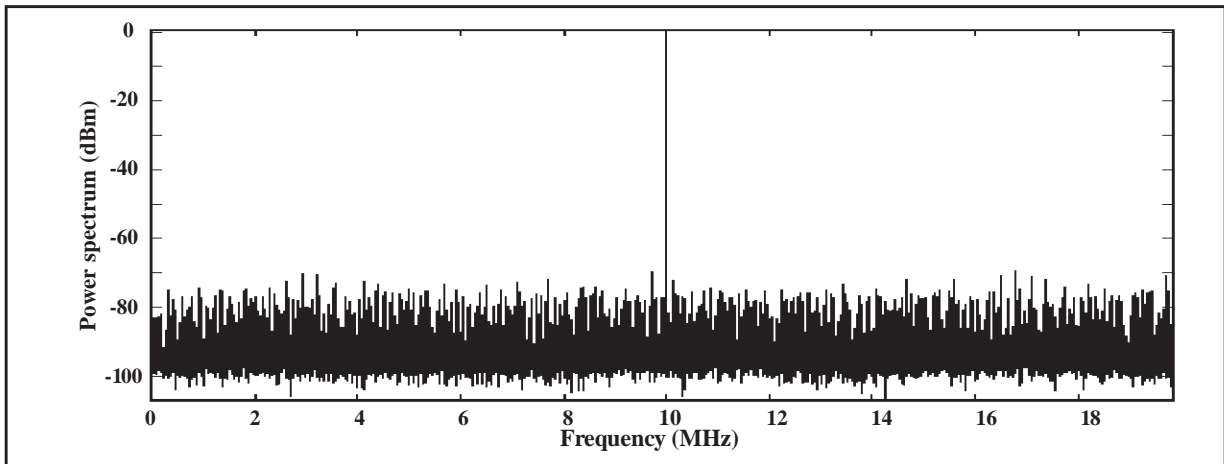


Power spectrum

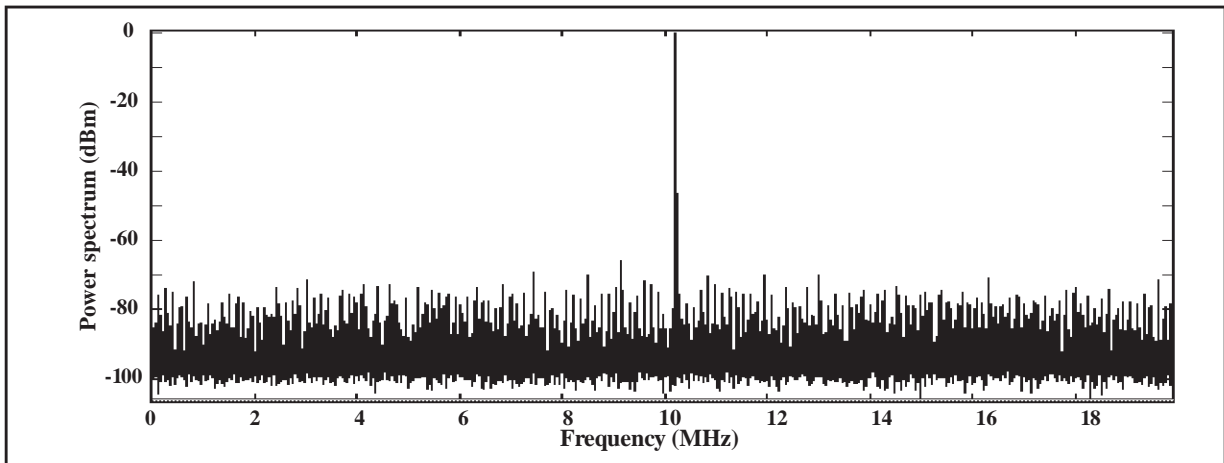
Fs=40MSPS - Icca=11mA - Fin=1MHz

**Power spectrum**

Fs=40MSPS - Icca=11mA - Fin=10MHz

**Power spectrum**

Fs=40MHz - Icca=11mA - Fin=50MSPS



TSA0801 APPLICATION NOTE

DETAILED INFORMATION

The TSA0801 is a High Speed analog to digital converter based on a pipeline architecture and the latest deep submicron CMOS process to achieve the best performances in terms of linearity and power consumption.

The pipeline structure consists of 9 internal conversion stages in which the analog signal is fed and sequentially converted into digital data.

Each 8 first stages consists of an Analog to Digital converter, a Digital to Analog converter, a Sample and Hold and a gain of 2 amplifier. A 1.5bit conversion resolution is achieved in each stage. The latest stage simply is a comparator. Each resulting LSB-MSB couple is then time shifted to recover from the conversion delay. Digital data correction completes the processing by recovering from the redundancy of the (LSB-MSB) couple for each

stage. The corrected data are outputted through the digital buffers.

Signal input is sampled on the rising edge of the clock while digital outputs are delivered on the falling edge of the Data Ready signal.

The advantages of such a converter reside in the combination of pipeline architecture and the most advanced technologies. The highest dynamic performances are achieved while consumption remains at the lowest level.

Some functionalities have been added in order to simplify as much as possible the application board. These operational modes are described in the following table.

The TSA0801 is pin to pin compatible with the 10bits/25Msps TSA1001, the 10bits/50Msps TSA1002 and the 12bits/50Msps TSA1201. This ensures a conformity within the product family and above all, an easy upgrade of the application.

OPERATIONAL MODES DESCRIPTION

Inputs				Outputs			
Analog input differential level			DFSB	OEB	OR	DR	Most Significant Bit (MSB)
(VIN-VINB)	>	RANGE	H	L	H	CLK	D9
-RANGE	>	(VIN-VINB)	H	L	H	CLK	D9
RANGE>	(VIN-VINB)	>-RANGE	H	L	L	CLK	D9
(VIN-VINB)	>	RANGE	L	L	H	CLK	Complemented D9
-RANGE	>	(VIN-VINB)	L	L	H	CLK	Complemented D9
RANGE>	(VIN-VINB)	>-RANGE	L	L	L	CLK	Complemented D9
X			X	H	HZ	HZ	HZ

Data Format Select (DFSB)

When set to low level (VIL), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing.

When set to high level (VIH), DFSB provides a standard binary output coding.

Output Enable (OEB)

When set to low level (VIL), all digital outputs remain active and are in low impedance state. When set to high level (VIH), all digital outputs buffers are in high impedance state. This results in lower consumption while the converter goes on sampling.

When OEB is set to low level again, the data is then valid on the output with a very short Ton delay.

The timing diagram summarizes this operating cycle.

Out of Range (OR)

This function is implemented on the output stage in order to set up an "Out of Range" flag whenever the digital data is over the full scale range.

Typically, there is a detection of all the data being at '0' or all the data being at '1'. This ends up with an output signal OR which is in low level state (VOL) when the data stay within the range, or in high level state (VOH) when the data are out of the range.

Data Ready (DR)

The Data Ready output is an image of the clock being synchronized on the output data (D0 to D9). This is a very helpful signal that simplifies the synchronization of the measurement equipment or the controlling DSP.

As digital output, DR goes in high impedance state when OEB is asserted to High level as described in the timing diagram.

DRIVING THE ANALOG INPUT

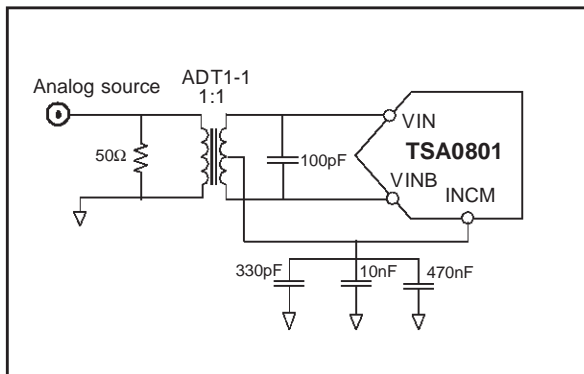
Differential inputs

The TSA0801 has been designed to obtain optimum performances when being differentially driven. An RF transformer is a good way to achieve such performances.

Figure 5 describes the schematics. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs. The common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set to 0.56V. The INCM is decoupled to maintain a low noise level on this node. Our evaluation board is mounted with a 1:1 ADT1-1 transformer from Minicircuits. You might also use a higher impedance ratio (1:2 or 1:4) to reduce the driving requirement on the analog signal source.

Each analog input can drive a 1Vpp amplitude input signal, so the resultant differential amplitude is 2Vpp.

Figure 5 : Differential input configuration



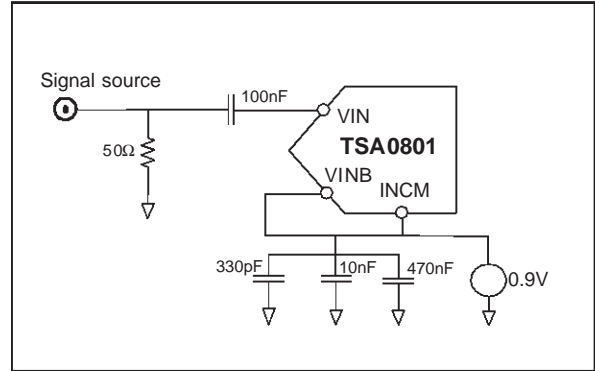
Single-ended input configuration

Some applications may require a single-ended input which is easily achieved with the configuration reported on Figure 6.

In this case, it is recommended to use an AC-coupled analog input and connect the other analog input to the common mode voltage of the circuit (INCM) so as to properly bias the ADC. The INCM may remain at the same internal level (0.56V) thus supporting only a 1Vpp of input

amplitude, or it must be increased to 0.9V to support a 2Vpp input amplitude. Performances are better when using a 2Vpp signal.

Figure 6 : Single-ended input configuration

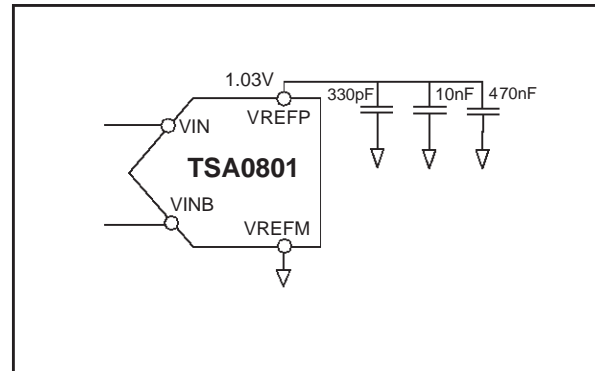


REFERENCE CONNECTION

Internal reference

In the standard configuration, the ADC is biased with the internal reference voltage. VREFM pin is connected to Analog Ground while VREFP is internally set to a voltage of 1.03V. It is recommended to decouple the VREFP in order to minimize low and high frequency noise. Refer to Figure 7 for the schematics.

Figure 7 : Internal reference setting

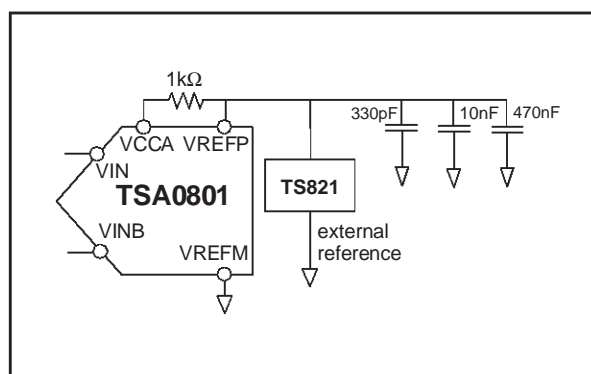


External reference

It is possible to use an external reference voltage instead of the internal one for specific applications requiring even better linearity or enhanced tem0801perature behavior. In this case, the amplitude of the external voltage must be at least equal to the internal one (1.03V). Using the STMicroelectronics Vref TS821 leads to optimum

performances when configured as shown on Figure 8.

Figure 8 : External reference setting



At 15MSPS sampling frequency, 1MHz input frequency and -1dBFS amplitude signal, performances can be improved of up to 2dBc on SFDR and 0.3dB on SINAD. At 40MSPS sampling frequency, 1MHz input frequency and -1dBFS amplitude signal, performances can be improved of up to 1dBc on SFDR and 0.6dB on SINAD.

This can be very helpful for example for multichannel application to keep a good matching among the sampling frequency range.

Clock input

The quality of your converter is very dependant on your clock input accuracy, in terms of aperture jitter; the use of low jitter crystal controlled oscillator is recommended.

The duty cycle must be between 45% and 55%.

The clock power supplies must be separated from the ADC output ones to avoid digital noise modulation at the output.

It is recommended to always keep the circuit clocked, even at the lowest specified sampling frequency of 0.5MSPS, before applying the supply voltages.

Power consumption optimization

The internal architecture of the TSA0801 enables to optimize the power consumption according to the sampling frequency of the application. For this purpose, a resistor is placed between IPOL and the analog Ground pins.

The TSA0801 will combine highest performances and lowest consumption at 40MSPS when Rpol is equal to 18kΩ.

At lower sampling frequency range (< 10MSPS), this value of resistor may be adjusted in order to decrease the analog current without any degradation of dynamic performances.

As an example, 10mW total power consumption is achieved at 5 MSPS with Rpol equal to 390kΩ.

The table below sums up the relevant data.

Total power consumption optimization depending on Rpol value

Fs (MSPS)	5	15	25	40
Rpol (kΩ)	390	40	25	18
Optimized power (mW)	10	25	35	40

Layout precautions

To use the ADC circuits in the best manner at high frequencies, some precautions have to be taken for power supplies:

- First of all, the implementation of 4 separate proper supplies and ground planes (analog, digital, internal and external buffer ones) on the PCB is mandatory for high speed circuit applications to provide low inductance and low resistance common return.

The separation of the analog signal from the digital part is essential to prevent noise from coupling onto the input signal.

- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.
- Proper termination of all inputs and outputs must be incorporated with output termination resistors; then the amplifier load will be only resistive and the stability of the amplifier will be improved. All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.

- To keep the capacitive loading as low as possible at digital outputs, short lead lengths of routing are essential to minimize currents when the output changes. To minimize this output capacitance, buffers or latches close to the output pins will relax this constraint.

- Choose component sizes as small as possible (SMD).

TSA0801

EVAL0801 evaluation board

The characterization of the board has been made with a fully ADC devoted test bench as shown on Figure 10. The analog signal must be filtered to be very pure.

The dataready signal is the acquisition clock of the logic analyzer.

The ADC digital outputs are latched by the octal buffers 74LCX573.

All characterization measurements have been made with:

SFSR=+0.2dB for static parameters.-
SFSR=-0.5dB for dynamic parameters.

Figure 9 : Analog to Digital Converter characterization bench

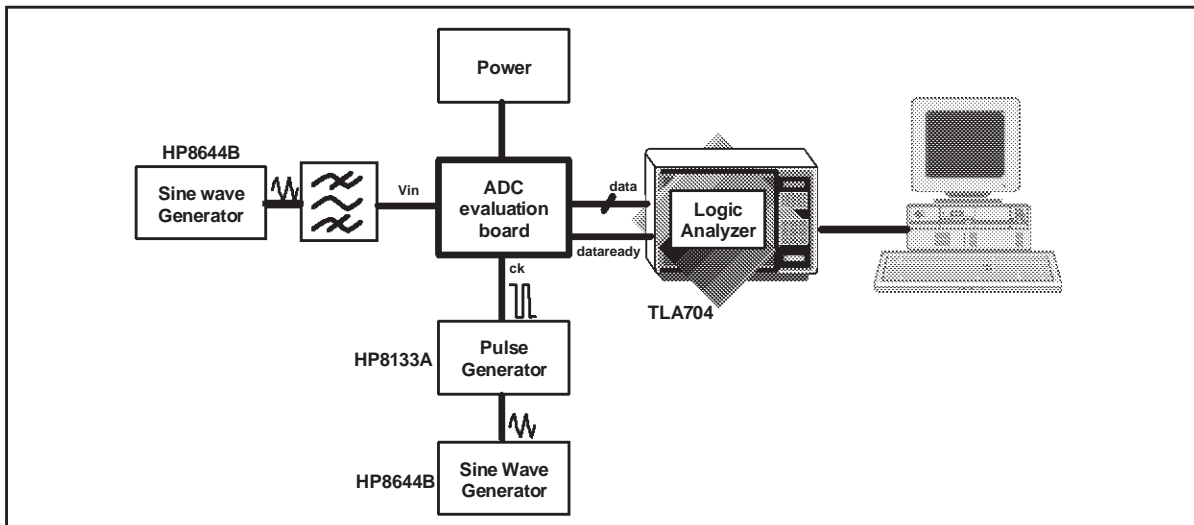


Figure 10 : TSA0801 evaluation board schematic

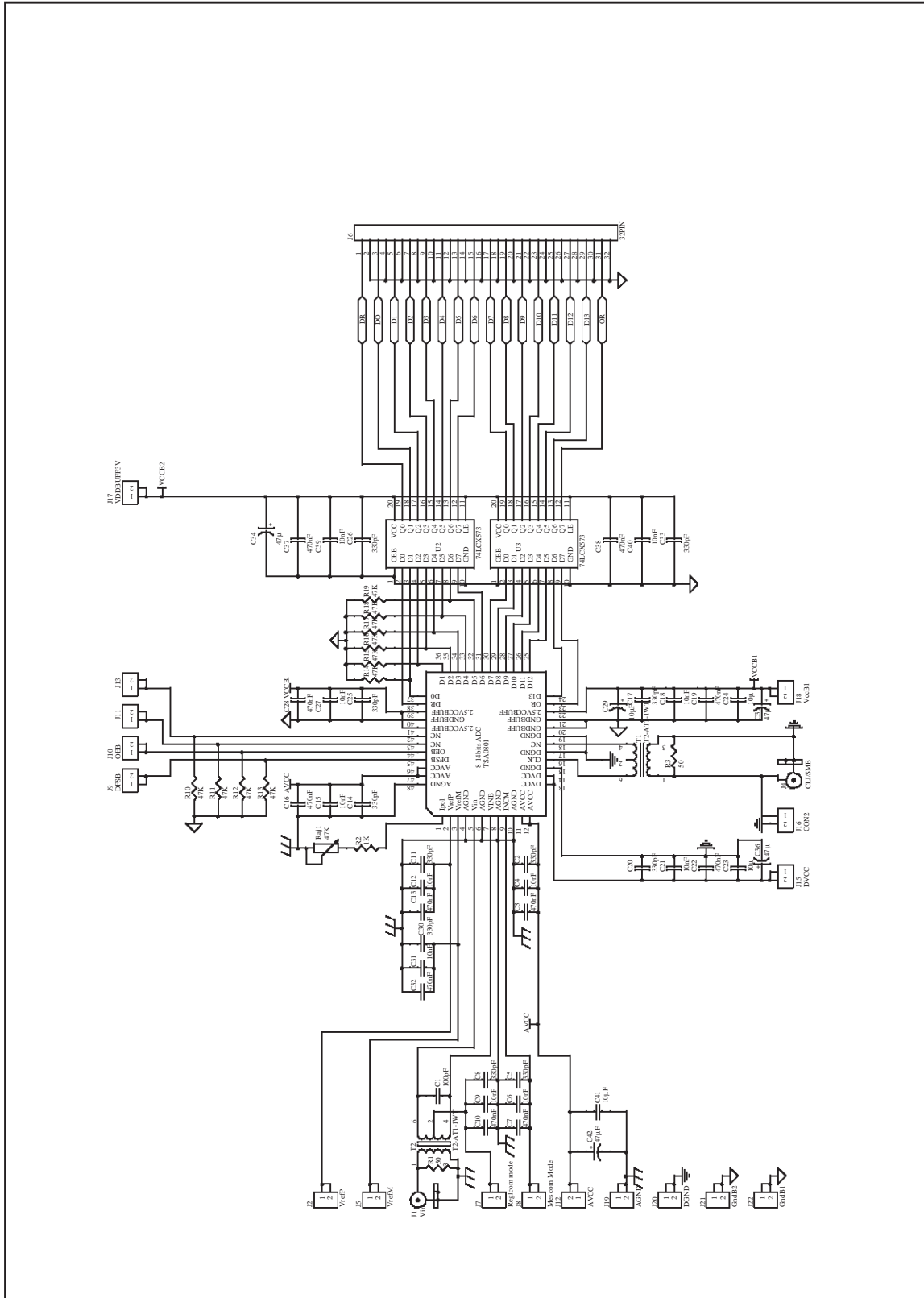
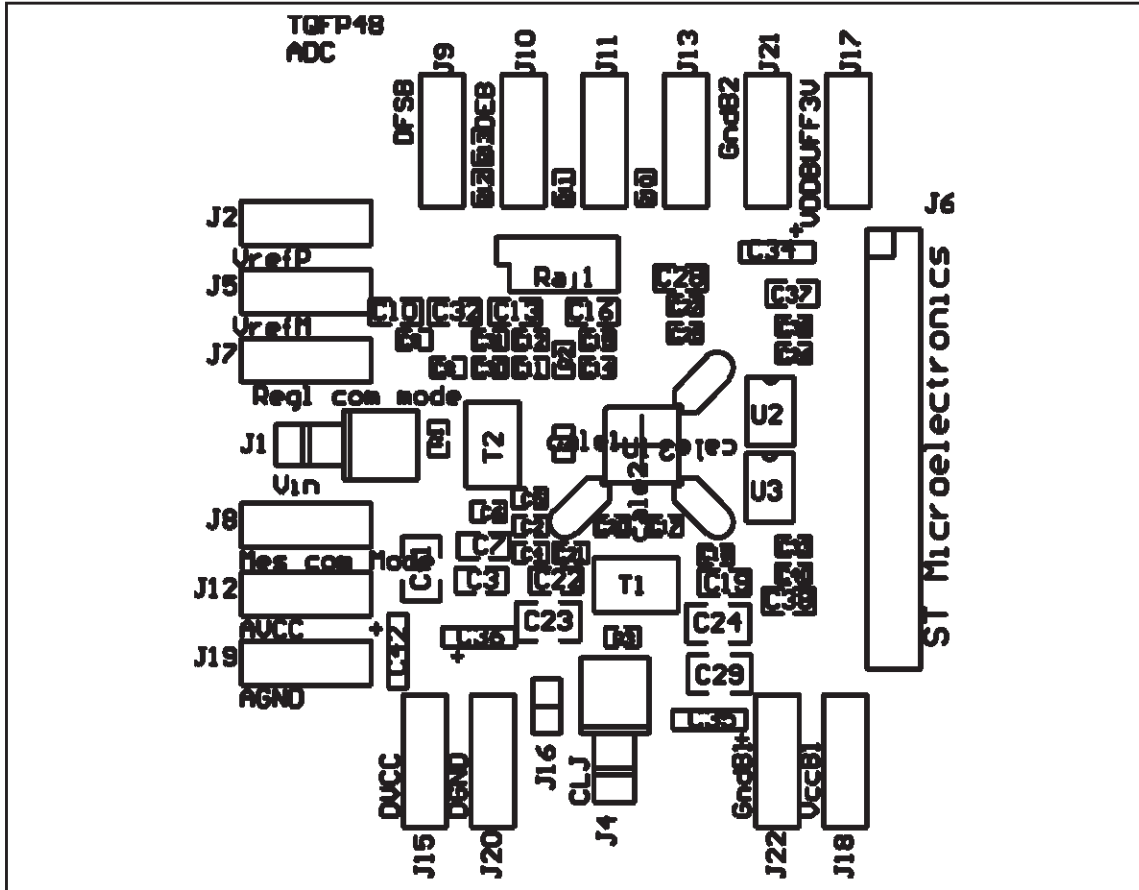


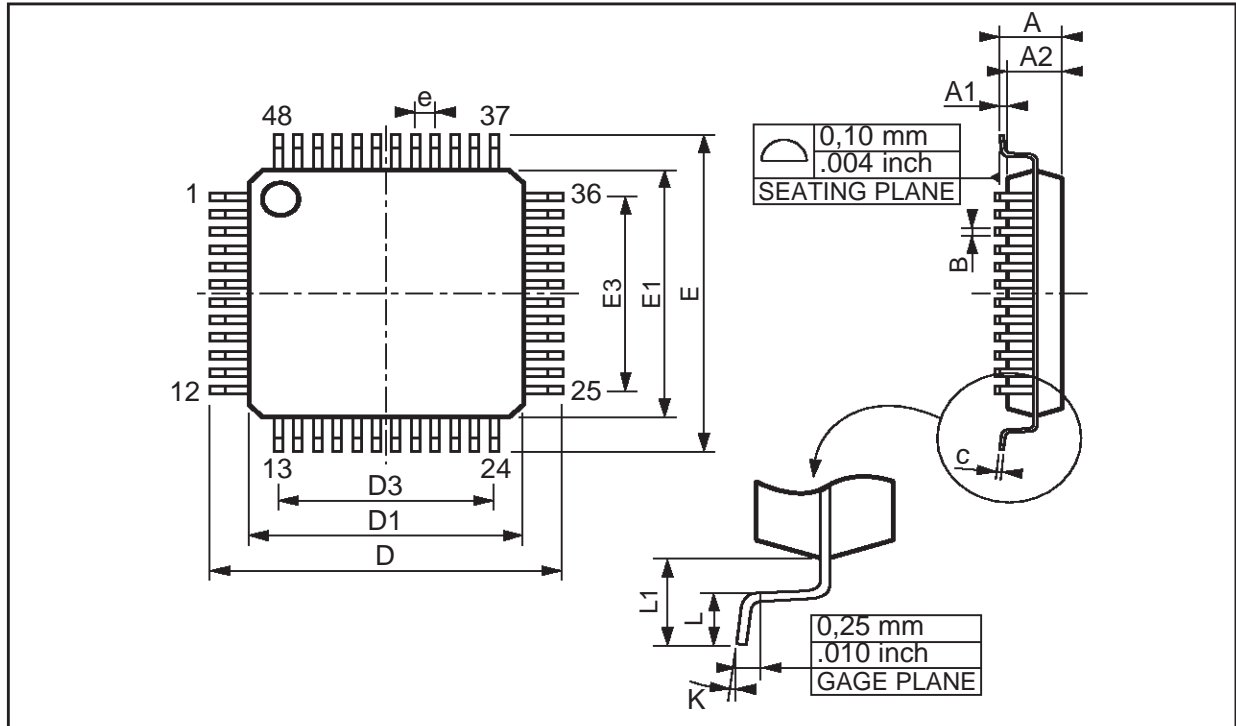
Figure 11 : circuit board - Top side silkscreen



Printed circuit board - List of components

Part	Design	Footprint	Part	Design	Footprint	Part	Design	Footprint	Part	Design	Footprint
Type	ator		Type	ator		Type	ator		Type	ator	
10uF	C 24	1210	330pF	C 33	603	470nF	C 7	805	AVCC	J12	FICHE2MM
10uF	C 23	1210	330pF	C 20	603	470nF	C 16	805	CLJ/SMB	J4	SMB/H
10uF	C 41	1210	330pF	C 8	603	470nF	C 19	805	AGND	J19	FICHE2MM
10uF	C 29	1210	330pF	C 2	603	470nF	C 3	805	DFSB	J9	FICHE2MM
100pF	C 1	603	330pF	C 5	603	47KΩ	R 12	603	DGND	J20	FICHE2MM
10nF	C 12	603	330pF	C 11	603	47KΩ	R 14	603	DVCC	J15	FICHE2MM
10nF	C 39	603	330pF	C 30	603	47KΩ	R 11	603	GndB1	J22	FICHE2MM
10nF	C 15	603	330pF	C 17	603	47KΩ	Raj1	VR 5	GndB2	J21	FICHE2MM
10nF	C 40	603	330pF	C 14	603	47KΩ	R 10	603	Mes com mode	J8	FICHE2MM
10nF	C 27	603	47uF	C 36	CAP	47KΩ	R 19	603	OEB	J10	FICHE2MM
10nF	C 4	603	47uF	C 34	CAP	47KΩ	R 13	603	Regl com mode	J7	FICHE2MM
10nF	C 21	603	47uF	C 35	CAP	47KΩ	R 15	603	T2-AT1-1WT	T2	ADT
10nF	C 31	603	47uF	C 42	CAP	47KΩ	R 16	603	T2-AT1-1WT	T1	ADT
10nF	C 6	603	470nF	C 22	805	47KΩ	R 17	603	VccB1	J18	FICHE2MM
10nF	C 9	603	470nF	C 32	805	47KΩ	R 18	603	VDDBUFF3V	J17	FICHE2MM
10nF	C 18	603	470nF	C 37	805	50Ω	R 3	603	Vin	J1	SMB/H
1KΩ	R 2	603	470nF	C 38	805	50Ω	R 1	603	VrefM	J5	FICHE2MM
32PIN	J 6	IDC 32	470nF	C 13	805	74LXX573	U3	TSSOP 20	VrefP	J2	FICHE2MM
330pF	C 25	603	470nF	C 28	805	74LXX573	U2	TSSOP 20	TSA0801	U1	TOFP48
330pF	C 26	603	470nF	C 10	805	C ON2	J16	SIP 2			

PACKAGE MECHANICAL DATA:
48 PINS - PLASTIC PACKAGE



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K						

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