NPC
NIPPON PRECISION CIRCUITS LTD.

PLL2001

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

■ General Description

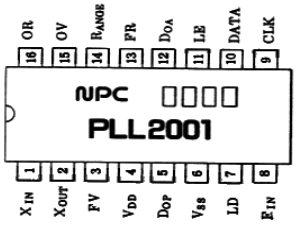
The PLL2001 is a CMOS LSI for PLL Frequency Synthesizer. 16bit programmable divide – by – R counter and divide – by – N counter are set by serial data.

■ Features

- 200MHz input capability (5V,typ,F_{IN})
- 20MHz input capability (5V,typ,X_{IN})
- ÷R range = 5 to 65535
- ÷N range = 272 to 65535
- Lock Detect signal
- Both Active and Passive filter can be use
- FV and FR signal output terminals
- Package 16PIN Dual – Inline – Plastic
  16PIN Small – Outline – Plastic

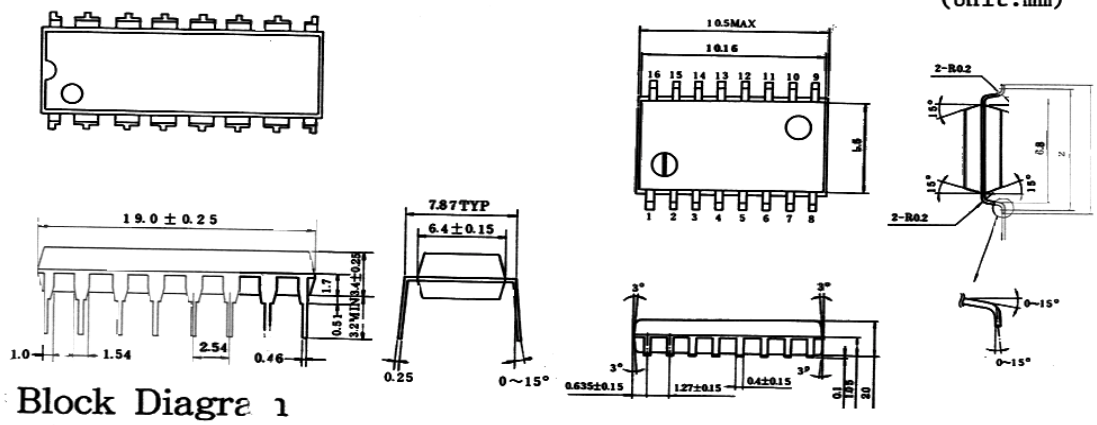
■ Pin Asignment

TOP VIEW

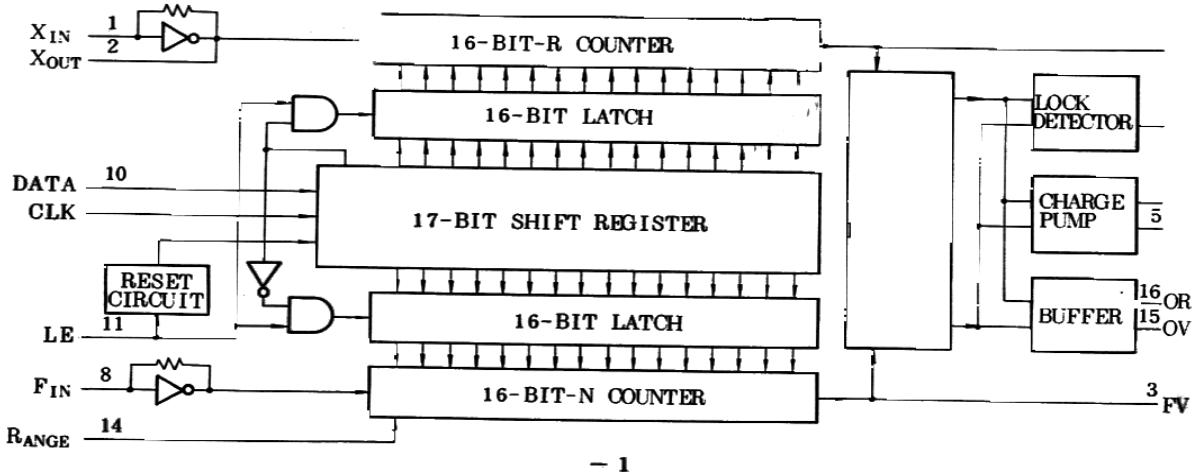


■ Package Dimension

(Unit:mm)



■ Block Diagram



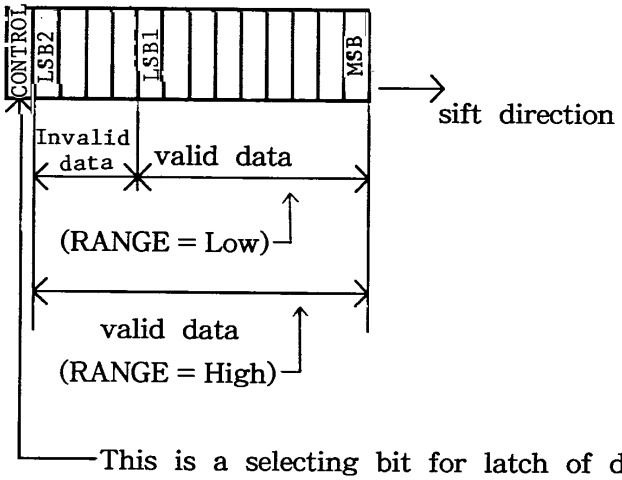
■ PIN Description (1 of 2)

PIN name	Function
XIN (1) XOUT (2)	These pins are connected to terminals of an external pallarel resonant crystal. XIN may also serve as input for an externaly-generated reference signal. It has feed back resistor, so that can use capacitance coupling. XOUT can be use for external circuit.
FV (3) FR (13)	There are buffered outputs from compare-divider (FV) and reference-divider (FR).
VDD (4)	Power supply (2.7~5.5V)
DOP (5) DOA (12) OV (15) OP (16)	There are terminals for low pass filter. DOP and DOA are tri-state outputs. These four outputs can be selected as follows. DOP : Passive filter DOA : Active filter OV, OR : Differential filter
VSS (6)	Ground
FIN (8) RANGE (14)	FIN is a input for compare-divider. It has feed back resistor, so that can use capacitance coupling. A input frequency range can be selected as follows, 1. RANGE is high A input range is 5MHz to 250MHz (typ @ 5.0V) 1.0V p-p sine wave. 2. RANGE is low A input range is DC to 22MHz (typ @ 5.0V) 1.5V p-p sine wave.

■ PIN Description (2 of 2)

PIN name	Function
DATA (10) CLK (9)	There are a data and a clock inputs to a sift register. A serial data sifts when CLK changes low to high. The structure of sift register and input data format refer to Fig 1.
LE (11)	This is a write signal to latch. When LE is held high, write mode is active. The sift register is cleared at the falling edge of LE.
LD (7)	This is a unlock detect terminal. When PLL is unlocked, LD becomes to be low.

Divide ratio of Compare – Divider and Reference – Divider



This is a selecting bit for latch of divide ratio

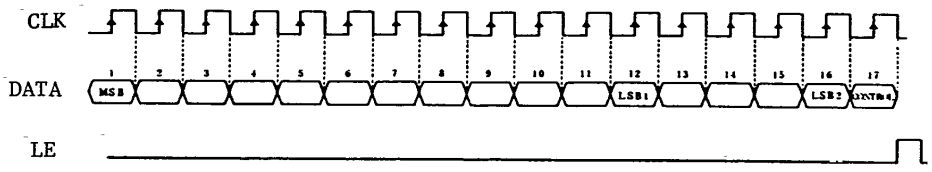
CONTROL = High → set a Reference – Divider

CONTROL = Low → set a Compare – Divider

When the all bits of N – latch (Compare-Divider) is cleared, stops count, thus current consumption decreases. When the all bits of R – latch (Reference - Divider) is cleared, the oscllator stops. The result of clear all bits of both N and R latch, a current consumption is within 10 μ A.

Fig1

■ Setting a Divide Ratio data



- A serial data must be input from MSB.
- A serial data is latched at the rising edge of CLK, thus data must change at falling edge of CLK.
- LE must be low while data are written to sift register. Data is trans－fer from sift register to Reference－Divider or Compare－Divider, when LE is held high.
- A sift register is cleared at the falling edge of LE. It is applicable to save a current consumption. (all bits are 0) (see fig2)

①Set CONTROL = High
Set another bits = Low

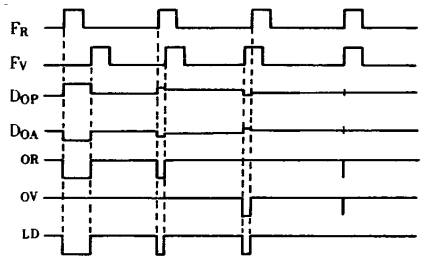
②Set all bits of Reference Divider = Low

③Clear sift register

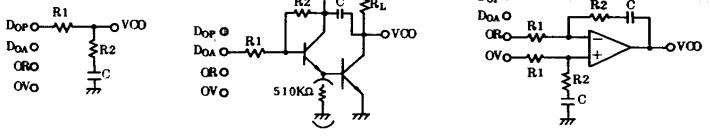
④Set all bits of Compare Divider = Low

Fig2

■ Phase Comparator timing chart



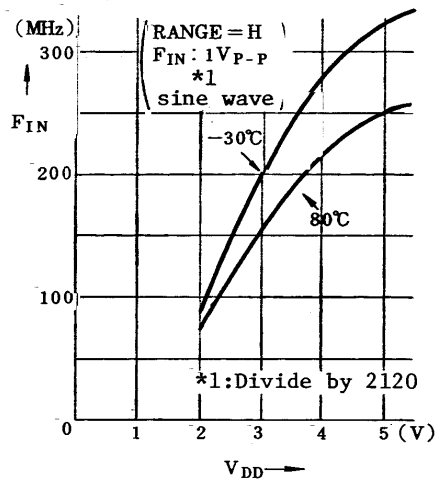
■ Low Pass Filter



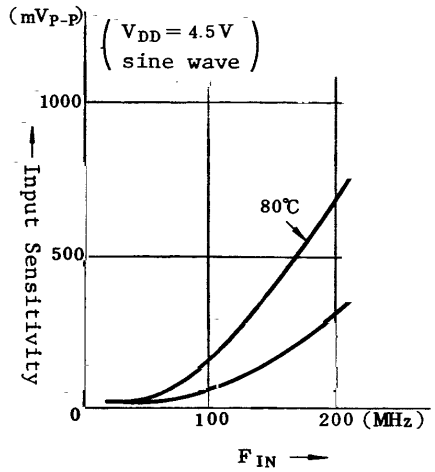
Passive filter Active filter Differential filter

■ Typical Specification

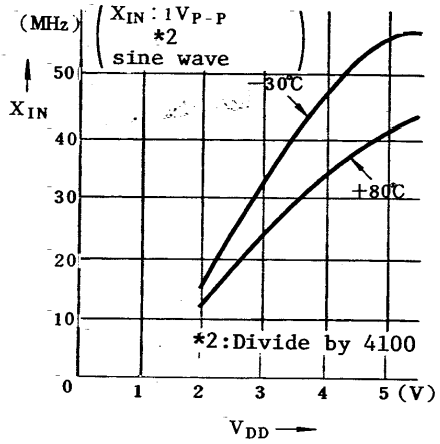
① F_{IN} Maximum Operating Frequency's Specification



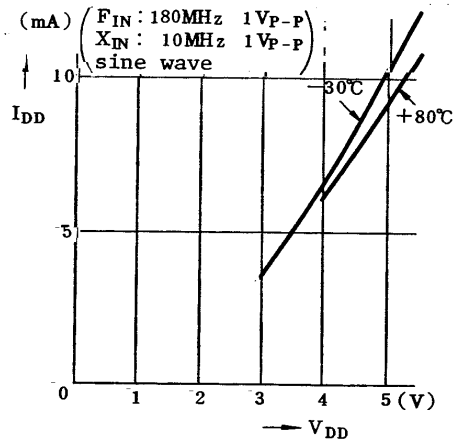
② F_{IN} Frequency-Input Sensitivity's Specification



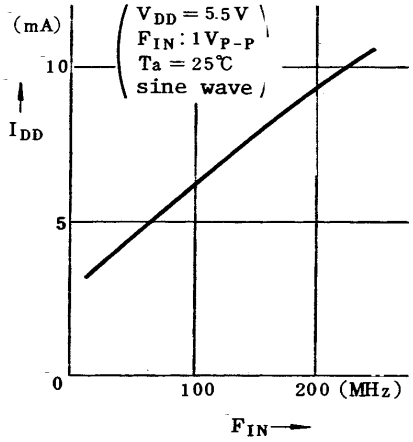
③ X_{IN} Maximum Operating Frequency's Specification



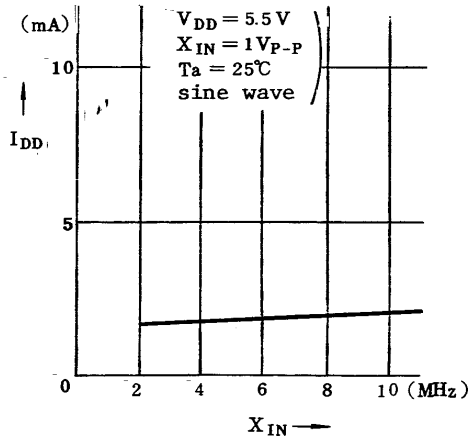
④ Supply Voltage(Vdd)- Current Consumption's Specification



⑤ F_{IN} Input Frequency- Current Consumption Specification



⑥ X_{IN} Input Frequency- Current Consumption's Specification



■ Electrical Characteristics

$V_{SS}=0V$ $T_a=-30\sim+80℃$

Parameter	Symbol	Conditions		Value			Units
		VDD(V)		min	typ	max	
Supply Voltage	VDD	-	-	2.7	-	5.5	V
Current Consumption	IDD1	2.7~3.3	FIN=60MHz, 1VP-P sine wave XIN=10MHz, 1VP-P sine wave	-	-	13	mA
		4.5~5.5	FIN=100MHz, 1VP-P sine wave XIN=10MHz, 1VP-P sine wave	-	-	25	mA
Stand-by Current	IDD2	2.7~5.5	R-Latch, N-Latch is all "0"	-	-	10	μA
Maximum Operating Frequency FIN	fmax1	2.7~3.3	FIN=1VP-P sine wave	60	140	-	MHz
		4.5~5.5	RANGE=HIGH	180	250	-	MHz
	fmax2	2.7~3.3	FIN=1.5VP-P sine wave	10	14	-	MHz
		4.5~5.5	RANGE=LOW	15	22	-	MHz
Frequency XIN	fmax3	2.7~3.3	XIN=1VP-P sine wave	11	14	-	MHz
		4.5~5.5		15	22	-	MHz
Minimum Operating Frequency	fmin	2.7~5.5	FIN=1VP-P sine wave RANGE=HIGH	-	-	5	MHz
			FIN=1VP-P sine wave RANGE=LOW	-	-	DC	MHz
Input Voltage Range FIN, XIN	VIN	2.7~5.5	XIN and FIN(RANGE=HIGH)	1.0	-	VDD	V
			FIN(RANGE=LOW)	1.5	-	VDD	V
Input Voltage Range CLK, DATA, LE	VIH	2.7~3.3		VDD-0.6	-	-	V
		4.5~5.5		VDD-1.0	-	-	V
	VIL	2.7~3.3		-	-	0.6	V
		4.5~5.5		-	-	1.0	V
Input Current XIN	IIH1	2.7~3.3	VIH=VDD	-	-	10	μA
		4.5~5.5	VIH=VDD	-	-	15	μA
	IIL1	2.7~3.3	VIL=0V	-	-	10	μA
		4.5~5.5	VIL=0V	-	-	15	μA
Input Current FIN	IIH1	2.7~3.3	VIH=VDD	-	-	60	μA
		4.5~5.5	VIH=VDD	-	-	100	μA
	IIL1	2.7~3.3	VIL=0V	-	-	60	μA
		4.5~5.5	VIL=0V	-	-	100	μA
Output Current FV, DOP, LD, DOA FR, OV, OR	IOH	2.7~3.3	VOH=VDD-0.3V	0.2	-	-	mA
		4.5~5.5	VOH=VDD-0.4V	0.4	-	-	mA
	IOL	2.7~3.3	VOL=0.3V	0.2	-	-	mA
		4.5~5.5	VOL=0.4V	0.4	-	-	mA
Set-up Time DATA→CLK, CLK→LE	tsu1	2.7~5.5	see Fig3(next page)	300	-	-	nS
	tsu2	2.7~5.5		300	-	-	nS
Hold Time	tH	2.7~5.5		300	-	-	nS

■ Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Power Suplly	VDD	-0.3～0.7	V
Input Voltage	VIN	GND-0.3～VDD+0.3	V
Operating Temperature	VOPR	-30～+80	℃
Storage Temperatue	TSTG	-40～+125	℃
Soldering Temperature	TSLD	260±5	℃
Soldering Time	tSLD	10.5±0.5	℃

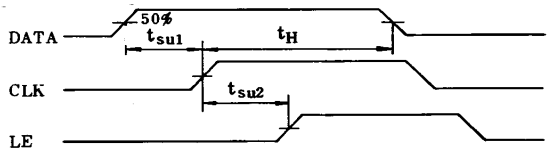


Fig3

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