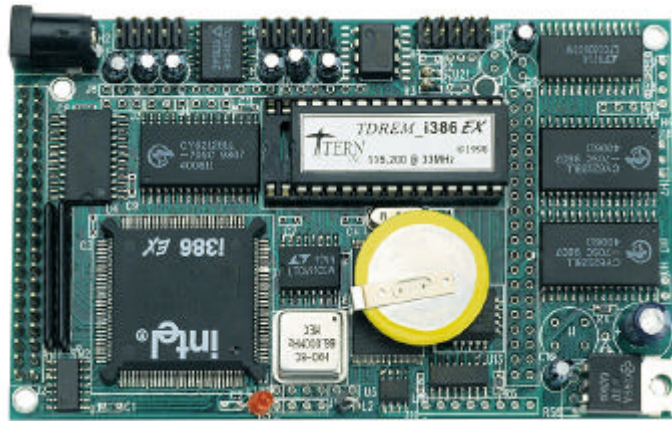
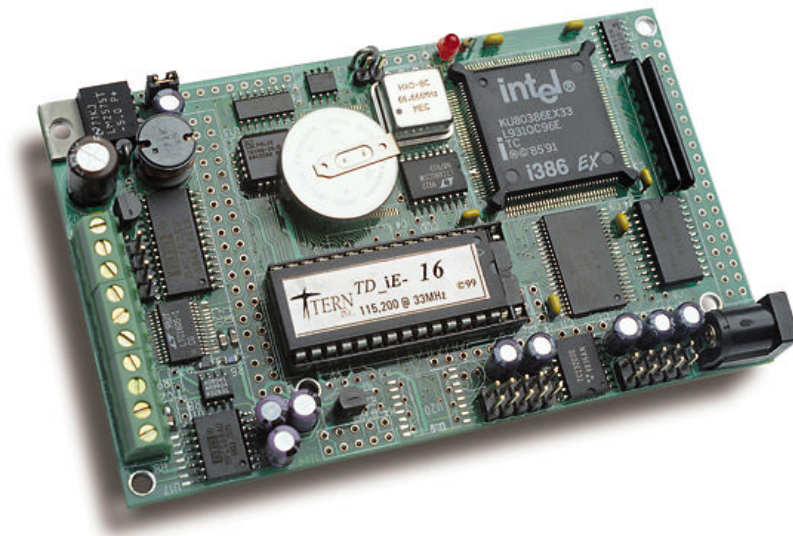


i386-Engine-P™



i386-Engine-M™



C/C++ programmable, 32-bit microprocessor module with
I/Os, UART, High-speed ADC
based on the Intel386EX

Technical Insert



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Supplement to i386-Engine ä Technical Manual

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Chapter 1: Introduction and Hardware

1.1 Introduction

The i386-Engine-P, or i386-Engine-M is based on the TERN i386-Engine™.

The “-P” version increases the memory to a total of 3 megabytes, including a 8-bit, up to 512KB SRAM (U1) and up to 1MB 16-bit SRAM made by two 8-bit SRAM chips (U17, U18). Only the 8-bit SRAM (U1) and the real-time clock can be battery backup. A 16-bit Flash 512KB (29F400) or 1MB (29F800) can be installed. There are no serial 11 channels slow 12-bit ADC, nor DACs on the “-P” while a single channel 16-bit 100K Hz ADC (LTC1605) can be installed.

The “-M” version supports one 16-bit SRAM, up to 512KB, and a 16-bit Flash 512KB (29F400) or 1MB (29F800). An optional 8 ch. 12-bit ADC (LTC1415, 1MHz, 0-4.096V) or 4 ch. 12/14-bit ADC (LTC1409/1419, 800K, ±2.5V), or 8 ch. 16-bit ADC (LTC1605-1, 100K, 0-4V) can be installed with an analog multiplexer (508, or 509) of 8 single-ended or 4 pair of differential inputs.

Both “-P” and “-M” version supports on-board switching power supply and RS232/485 drivers.

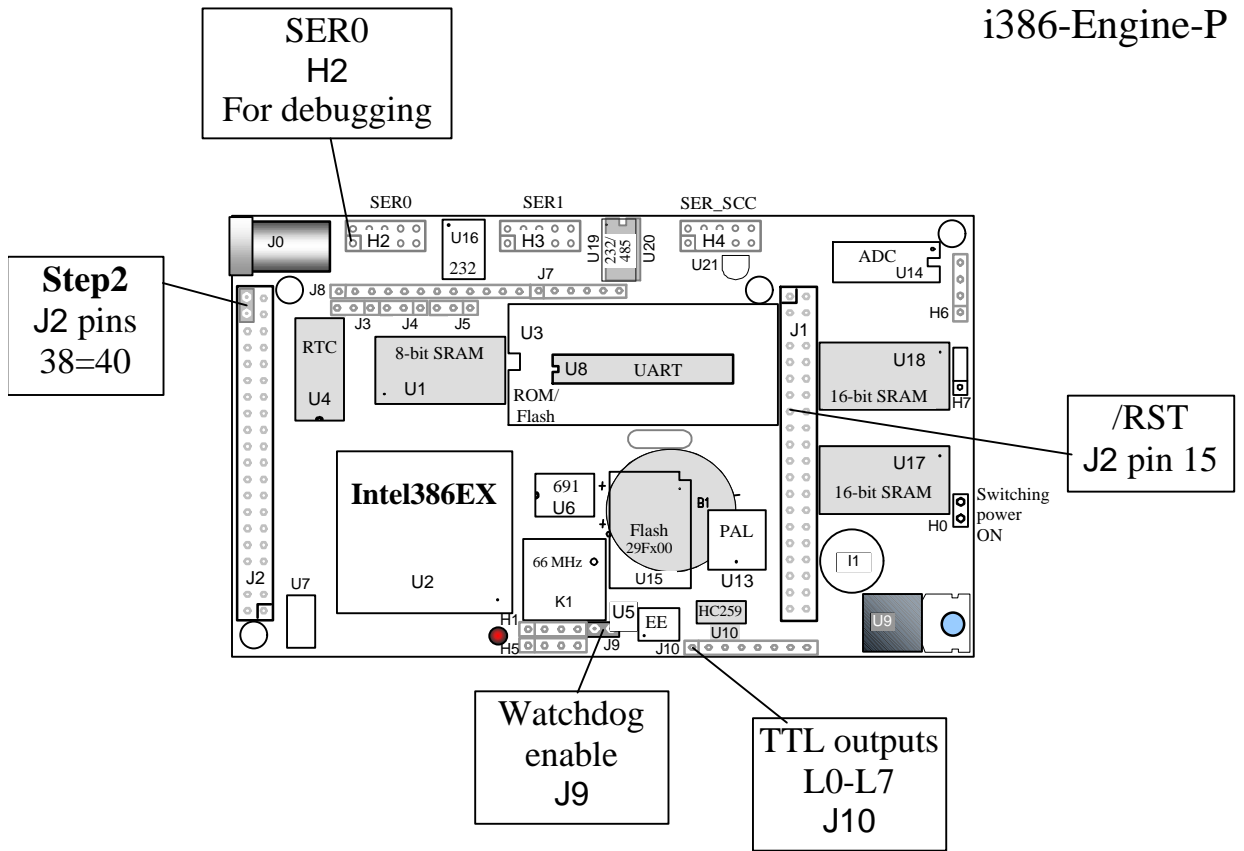


Figure 1.1 Physical layout of the i386-Engine-P

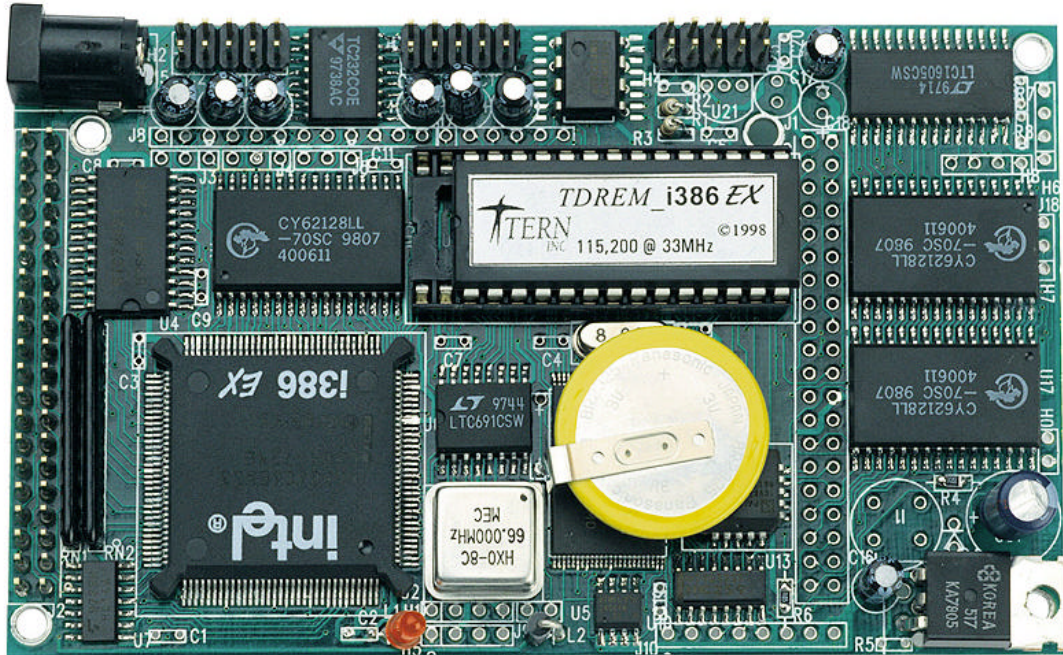


Figure 1.2 Photo of the i386-Engine-P™

The *i386-Engine-P™* (*IE-P*) is based on the *i386-Engine™* design, including on-board regulator, RS-232/485 drivers, single high speed ADC, and more on-board memory. In addition to 512 KB 8-bit SRAM and 512 KB 8-bit ROM/Flash, the *IE-P* supports up to 1 MB 16-bit SRAM and 1 MB 16-bit Flash. A 16-bit ADC (LTC1605, 100 KHz, ± 10 V), or a 12-bit ADC (LTC1415, 1.2 MHz, 0-5V) can be installed. The eight TTL outputs are designed for operating and external analog multiplexer for the single-channel ADC. The *IE-P* can be installed with *MC2140™*, *LittleDrive O*, *MemCardA™*, *MotionC™*, *P100 O*, or *P300 O*.

i386-Engine-P Features:

Features exclusive to the i386-Engine-P (i.e. not available on the i386-Engine) are shown in bold.

Standard Features:

- Dimensions: 4.5 x 2.7 x 0.3 inches
- Easy to program in C/C++
- Power consumption:
 - 300mA at 6.5V
 - 160mA at 12V
 - 80mA at 24V
 - 30mA at 30V
- Power input: +8.5V to +12 V unregulated DC with linear regulator
or, +8.5 to +35V unregulated DC with switching regulator (optional)
- Temperature: -40°C to +80°C
- 32-bit CPU (Intel i386EX), PC-compatible, C/C++ programmable
- A total of 64MB memory space, with 16 data lines and 26 address lines
- Two PC-compatible asynchronous serial ports and one synchronous serial port
- **Two RS-232 drivers**
- Three 8-bit I/O ports with multiplexed functions from i386EX
- **8 additional digital outputs**
- **Ports for three SRAM chips and two Flash chips:**

Up to 512KB Flash/ROM (socket); **up to 512KW SMT Flash**

- Three 16-bit timer/counters
- 512-byte serial EEPROM
- Up to 10 external interrupts and 8 internal interrupts
- Supervisor chip (691) for power failure, reset and watchdog
- Two DMA channels for data transfer between memory and I/O
- Up to 420 MB memory expansion with PCMCIA via the **MemCard-A**

Optional Features:

- **SRAM support:**
Three 8-bit SRAM ports each support 32x1KB, 128x1KB, or 512x1KB SRAM
- SCC2691 UART (on-board), with RS-232 or RS-485 drivers, supports 8-bit or 9-bit networking
- **Flash support:**
Socket supports 8-bit Flash or ROM for 32x1KB, 128x1KB or 512x1KB
Surface-mount supports 16-bit Flash: 256KW or 512KW
- Real-time clock RTC72423, lithium coin battery
- **On-board switching power regulator**
- **1 channel of 16-bit high speed ADC, sample rate up to 100 KHz**

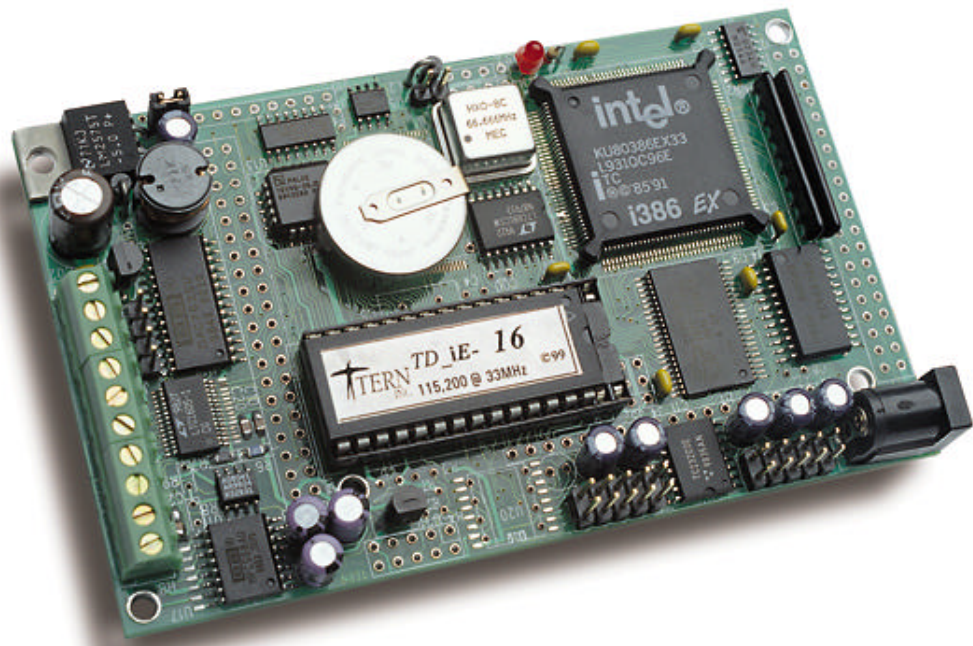


Figure 1.3 Photo of the i386-Engine-M

i386-Engine-M Features:

- Same mechanical and electrical as i386-Engine-P
- Single 16-bit SRAM replaces all 8-bit SRAM chips of IE-P
- Multiplexer (8 single or 4 differential) for analog inputs
- Optional 12/14/16-bit high speed parallel ADC*

- Optional 4 channels of 5 μ s 12-bit DAC(7625, BB)*

The *i386-Engine-M™ (IE-M)* is an enhanced version of the IE-P with same mechanical and electrical features. *IE-M* is an excellent high performance controller for high speed data acquisition and motion control.

A single 16-bit SRAM chip replaces all 8-bit SRAM chips of the IE-P. The 16-bit SRAM with battery backup and the 16-bit FLASH allow i386EX operating with external 16-bit data bus for code execution and data access. A 16-bit SRAM of 128KB or 512KB must be installed.

An optional 8 ch. 12-bit ADC (LTC1415, 1MHz, 0-4.096V) or 4 ch. 12/14-bit ADC (LTC1409/1419, 800K, \pm 2.5V), or 8 ch. 16-bit ADC (LTC1605-1, 100K, 0-4V) can be installed with an analog multiplexer (508, or 509) of 8 single-ended or 4 pair of differential inputs. A high speed 12-bit DAC7625 contains four precision output buffer amplifiers, providing 3 μ s output setting time and outputs 0 to 2.5V with an external 2.5V reference.

1.2 Connecting the i386-Engine-P, or i386-Engine-M to the PC

The following diagram (Figure 1.2) illustrates the connection between the i386-Engine-P and the PC. The i386-Engine-P is linked to the PC via a serial cable (PC-V25).

The *TDREM_i386EX* DEBUG ROM communicates through SER0 by default. Install the 5x2 IDE connector on the SER0 header (H2). **IMPORTANT:** Note that the red side of the cable must point to pin 1 of the H2 header. The DB9 connector should be connected to one of your PC's COM Ports (COM1 or COM2).

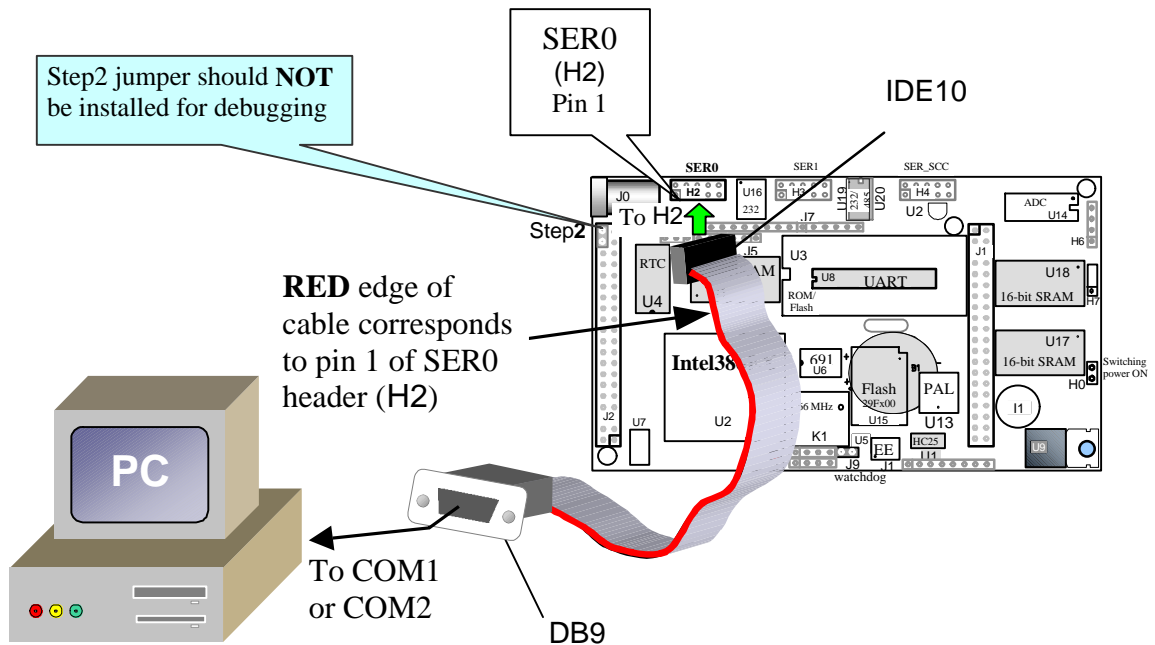


Figure 1.2 Figure 1.4 Connecting the i386-Engine-P to the PC

1.3 “-P” version Hardware

1.3.1 Three Megabyte Memory Mapping

Chip select lines for additional memory:

Memory Component	Chip Select Line
1MB Flash	CS1 = P21
16-bit SRAM (2 chips)	CS2

See `C:\TERN\386\SAMPLES\IE\IEP_RAM.C` for more information.

1.3.2 LTC1605 High Speed 16-bit ADC

The LTC1605 (U14) is a 100 ksp/s, sampling 16-bit A/D converter that draws only 55 mW from a single 5V supply. This device includes sample-and-hold, precision reference, switched capacitor successive approximation A/D and trimmed internal clock.

The LTC1605 has an industry standard $\pm 10V$ input range. Maximum DC specs include ± 2.0 LSB INL and 16-bit no missing codes over temperature. An external reference can be used if greater accuracy is needed. The ADC has a microprocessor compatible, 16-bit or two-byte parallel output port. The ID uses T6 to control the ADC's R/C pin and directly interface the full 16-bit data bus for maximum data transfer rate. The LTC1605 requires 8 μs AD conversion time. The busy signal has an 8 μs low period indicating the conversion in process.

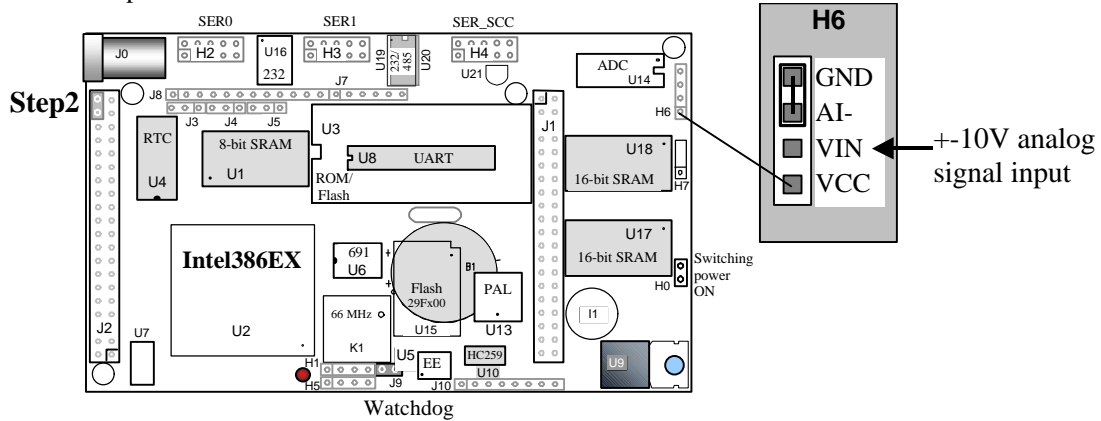


Figure 1.3 Figure 1.5 H6 header for ADC

In order to get the 100 KHz sample rate, The IE-P can not use interrupt operation to acquire data. A polling method is demonstrated in the sample program `id_ad16.c` located in the `c:\tern\386\samples\id` directory.

Pin Label	Location	Description
Vin	H6.2	Analog input. Full scale input range is $\pm 10V$.
AI-	H6.3	Analog ground plane.

Sample programs for the IE-P are listed in the `c:\tern\386\samples\iep` directory.

Please refer to the *i386-Engine Technical Manual* for information on all other components.

1.4 “-M” version Hardware

1.4.1 16-bit Fast SRAM

Only single 16-bit SRAM chip can be installed on the i386-Engine-M. /CS2 chip select line is used for the 16-bit SRAM up to 512KB or 256 KW memory:

Memory Component	Chip Select Line
16-bit SRAM, 0x0000-0x7fff	CS2

512KB 16-bit SRAM KM6164000-7L (Samsung) or 128KB 16-bit SRAM KM6161000-7L(Samsung) can be installed with using 1 wait state. Fast 16-bit SRAM CY7C1041-20 (Cypress, 512KB, 20 ns) or CY7C1021-20 (Cypress, 128KB, 20 ns) can be installed using zero wait state.

1.4.2 LTC1605-1 16-bit ADC(100KHz) or LTC1415 12-bit ADC(1.2 MHz)

The LTC1605-1 (U14) is a 100 ksp/s, sampling 16-bit A/D converter that draws only 55 mW from a single 5V supply. The LTC1605-1 has an 0 to 4V input range. This device includes sample-and-hold, precision reference, switched capacitor successive approximation A/D and trimmed internal clock. Maximum DC specs include ±2.0 LSB INL and 16-bit no missing codes over temperature. The ADC has a microprocessor compatible, 16-bit parallel output port. The IE-M uses T6 to control the ADC’s R/C pin and directly interface the full 16-bit data bus for maximum data transfer rate.

The LTC1605-1 requires 8 μs AD conversion time. The busy signal has an 8 μs low period indicating the conversion in process. The LTC1605-1 can be installed in U014.

The LTC1415 is a 1.25MHz, 12-bit ADC with 12-bit parallel interface using D15-D4 data lines of the i386EX. The LTC1415 has an 0 to 5V input range. It can be installed in U14.

The U014 and U14 are using two SSOP28 pads overlapped. Only one ADC can be installed at a time.

A 8-to-1 single-ended multiplexer (508, by default) can be installed in U017, or a 4-to-1 differential multiplexer (509) can be installed in U17.

The U017 and U17 are using two SOP16 pads overlapped. Only one ADC can be installed at a time.

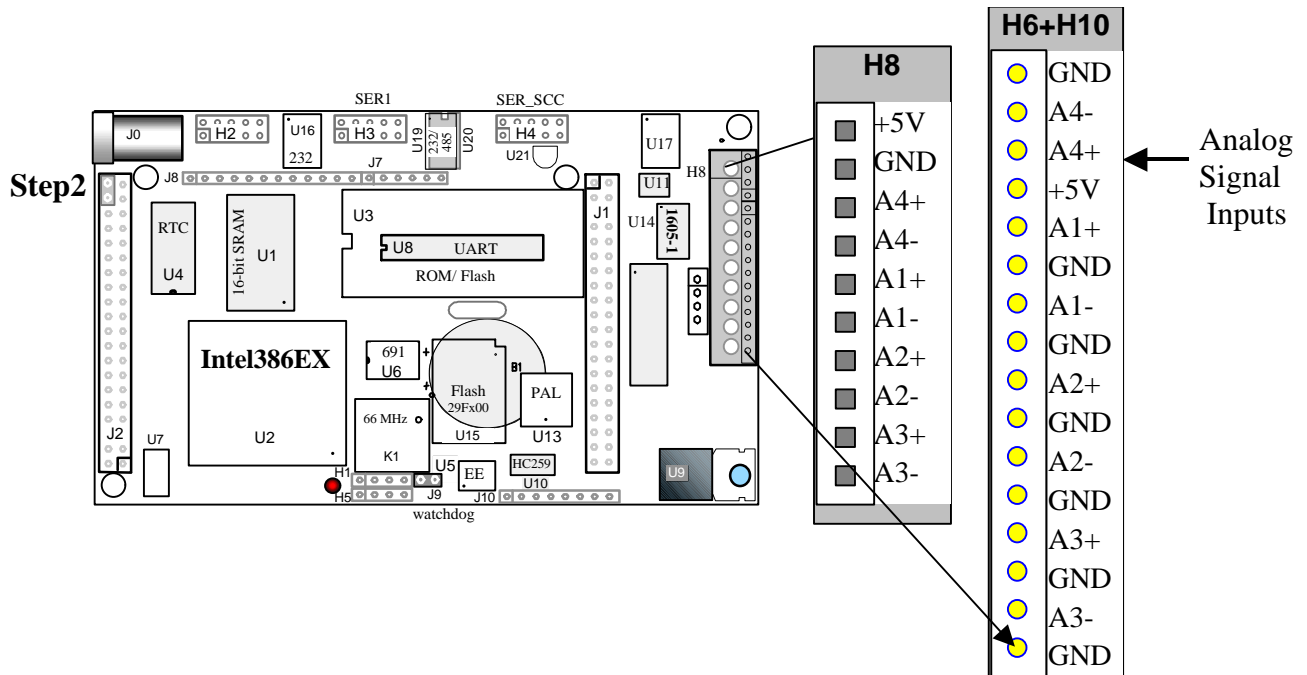


Figure 1.4 H8 screw terminals or H6+H10 headers for ADC inputs

A sample program `iem_ad16.c` located in the `c:\tern\386\samples\iep` directory.

H8 Pin Label	Screw Terminal	Description
VCC	H8.1	Regulated 5V
GND	H8.2	Ground
A4+	H8.3	Mux 508 analog input ch. 4 or Mux 509 ch. 4+
A4-	H8.4	Mux 508 analog input ch. 8 or Mux 509 ch. 4-
A1+	H8.5	Mux 508 analog input ch. 1 or Mux 509 ch. 1+
A1-	H8.6	Mux 508 analog input ch. 5 or Mux 509 ch. 1-
A2+	H8.7	Mux 508 analog input ch. 2 or Mux 509 ch. 2+
A2-	H8.8	Mux 508 analog input ch. 6 or Mux 509 ch. 2-
A3+	H8.9	Mux 508 analog input ch. 3 or Mux 509 ch. 3+
A3-	H8.10	Mux 508 analog input ch. 7 or Mux 509 ch. 3-

Table 1.1 H8 screw terminal signals

Pin Header Signal	H10	H6	Description
GND		4	Ground
A4-		3	Mux 508 analog input ch. 8 or Mux 509 ch. 4-
A4+		2	Mux 508 analog input ch. 4 or Mux 509 ch. 4+
VCC		1	Regulated 5V
A1+	1		Mux 508 analog input ch. 1 or Mux 509 ch. 1+
GND	2		
A1-	3		Mux 508 analog input ch. 5 or Mux 509 ch. 1-
GND	4		
A2+	5		Mux 508 analog input ch. 2 or Mux 509 ch. 2+
GND	6		
A2-	7		Mux 508 analog input ch. 6 or Mux 509 ch. 2-
GND	8		
A3+	9		Mux 508 analog input ch. 3 or Mux 509 ch. 3+
GND	10		
A3-	11		Mux 508 analog input ch. 7 or Mux 509 ch. 3-
GND	12		

Table 1.2 H6 and H10 pin header signals

Sample programs for the IE-M are listed in the `c:\tern\386\samples\iep` directory.

Please refer to the *i386-Engine Technical Manual* and i386-Engine-M schematics attached at the last page of this manual for more information.

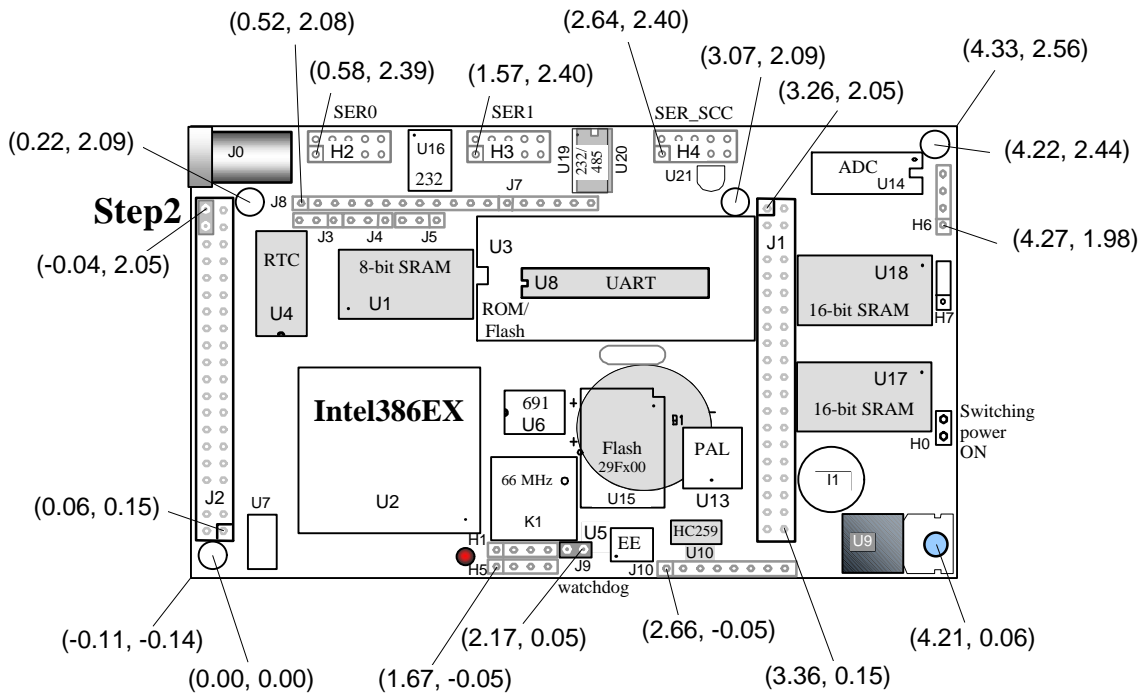


Figure 1.5 i386-Engine-P Layout

The i386-Engine-P/M measures 4.5 by 2.7 inches. All dimensions shown are in inches.

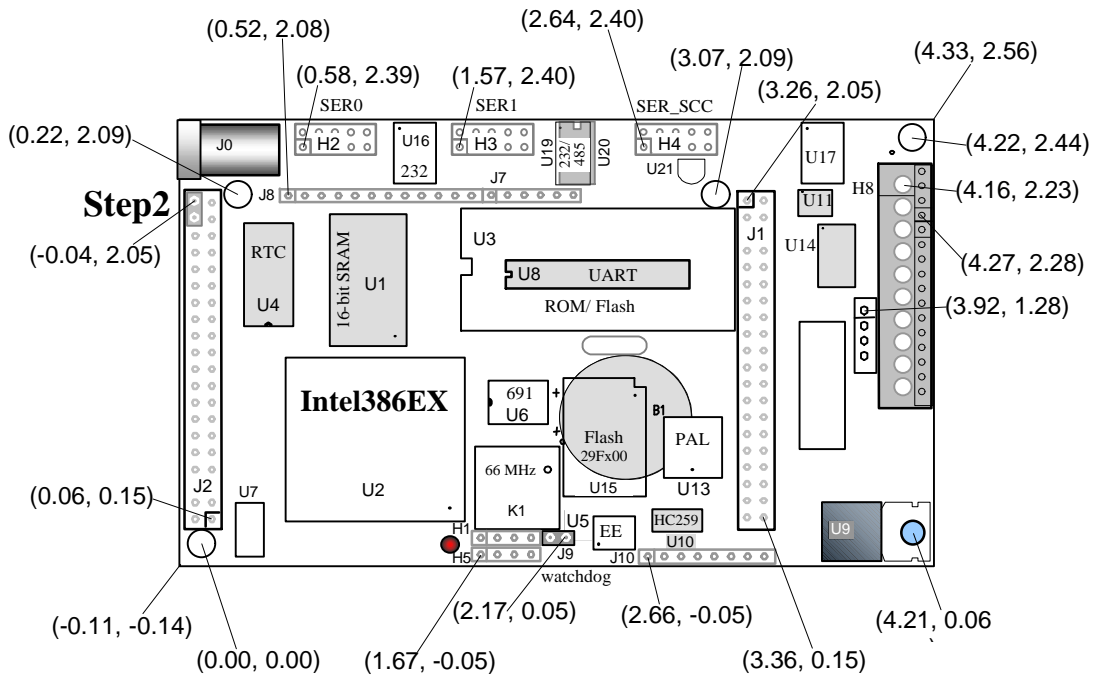


Figure 1.6 i386-Engine-M Layout

Chapter 2: 16-bit Flash/RAM Programming

The TERN i386-Engine-P/M (IE-P/M) and i386-Drive (ID) support 16-bit Flash and 16-bit RAM. The TERN ACTF Flash Kit now supports on-board programming/execution of the 16-bit Flash.

2.1 Minimum Requirements

- TERN Development Kit (DV-Kit)
- ACTF Flash Kit
- i386-Engine-P/M or i386-Drive with 256K Flash and 256K RAM
- TD_IE_16 Debug ROM

TD_IE_16 32K	0xFFFFF
	0xF8000
16-bit Flash 256K	0x81FFF
	0x80000
16-bit SRAM 512K	0x7FFFF
	0x00000

Figure 2.1 TD_IE_16 memory mapping configuration

2.2 Memory Mapping

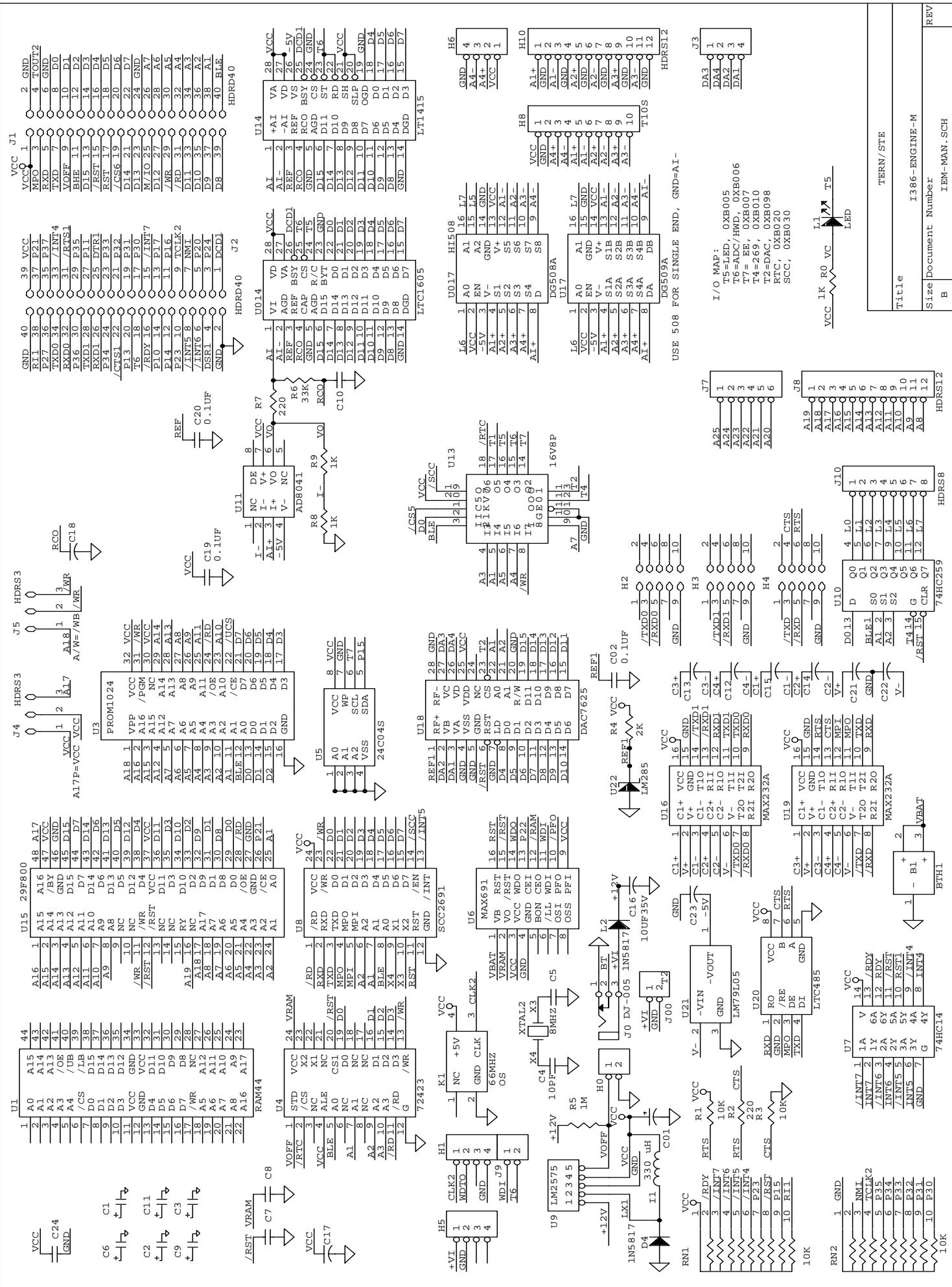
Memory for the 16-bit Flash configuration is shown in 0. The TD_IE_16 Debug ROM is located at the top of the memory map and is the first block to execute after power-on/reset. At power-on/reset, TD_IE_16 selects the dual chip 16-bit SRAM as memory.

2.2.1 Generating a HEX File

You must modify the MAKEFILE to generate a HEX for the 16-bit Flash. Modify the BOARD flag to IEP16 or ID16 respectively. Use the flash512.rm configuration file when generating HEX files. See the ACTF Flash Kit manual for the rest of the details about generating a HEX file.

2.2.2 Downloading a HEX file into the 16-bit Flash

Be sure that the step 2 address is set up correctly. If you are not sure, run **step2.c** in the debugger.



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