

FEATURES

- 65 MSPS sample rate
- 80 dBFS signal-to-noise ratio
- Transformer-coupled analog input
- Single PECL clock source
- Digital outputs
 - True binary format
 - 3.3 V and 5 V CMOS compatible

APPLICATIONS

- Low signature radar
- Medical imaging
- Communications instrumentation
- Instrumentation
- Antenna array processing

FUNCTIONAL BLOCK DIAGRAM

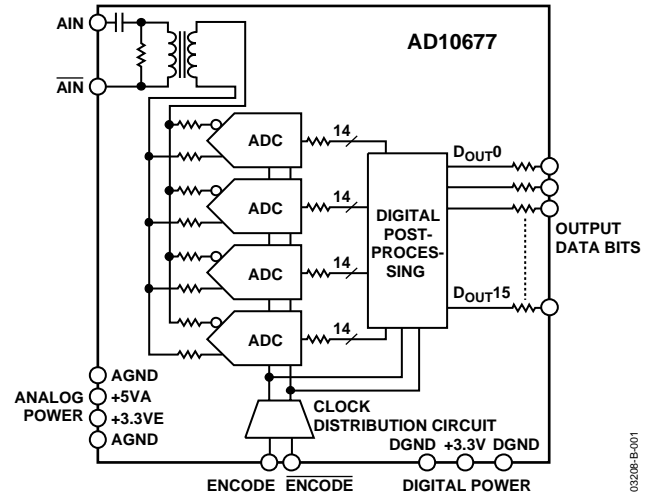


Figure 1

GENERAL DESCRIPTION

The AD10677 is a 16-bit, high performance, analog-to-digital converter for applications that demand increased SNR levels. Exceptional noise performance and a typical signal-to-noise ratio of 80 dBFS are obtained by digitally postprocessing the outputs of four ADCs. A single analog input and PECL sampling clock are required as well as 3.3 V and 5 V power supplies.

The AD10677 is assembled using a 0.062" thick laminate board with three sets of connector interface pads to accommodate analog and digital isolation. Analog Devices recommends using the FSI-110-03-G-D-AD-K-TR connector from Samtec. The overall card fits a 2.2" x 2.8" PCB specified from 0°C to 70°C.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 65 MSPS.
2. Input signal conditioning with optimized noise performance.
3. Fully tested and guaranteed performance.

Rev. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

| | | | |
|---------------------------------|---|---|----|
| Features | 1 | Absolute Maximum Ratings | 6 |
| Applications..... | 1 | Operating Range | 6 |
| General Description | 1 | ESD Caution | 6 |
| Functional Block Diagram | 1 | Test Circuits..... | 7 |
| Product Highlights | 1 | Typical Performance Characteristics | 10 |
| Revision History | 2 | Definition of Specifications | 11 |
| AD10677–Specifications | 3 | Thermal Considerations | 12 |
| DC Specifications | 3 | Theory of Operation..... | 12 |
| Digital Specifications | 4 | Analog and Digital Grounding | 13 |
| AC Specifications | 4 | Outline Dimensions | 19 |
| Switching Specifications | 5 | Ordering Guide | 20 |
| Explanation of Test Levels..... | 5 | | |

REVISION HISTORY

12/03—Data sheet changed from REV. A to REV.B

| | |
|---------------------------------------|-----------|
| Updated format..... | Universal |
| Changes to Table 1 and footnotes..... | 3 |
| Changes to Theory of Operation..... | 12 |
| Changes to Ordering Guide | 20 |

8/03—Data sheet changed from REV. 0 to REV. A

| | |
|---|----|
| Changes to Specifications | 2 |
| Changes to Table 1..... | 4 |
| Changes to Definition of Specifications | 10 |
| Updated Outline Dimensions | 18 |

AD10677—SPECIFICATIONS

DC SPECIFICATIONS

Table 1. $AV_{CC} = 5\text{ V}$, $EV_{CC} = 3.3\text{ V}$, $V_{DD} = 3.3\text{ V}$; $T_A = 25^\circ\text{C}$, Differential Encode = 65 MSPS, $C_{LOAD} \leq 10\text{ pF}$, unless otherwise noted.

| Parameter | Test Level | Min | Typ | Max | Unit |
|--|------------|-------|-----------|-------|-----------------------|
| RESOLUTION | | | 16 | | Bits |
| Offset Error | I | -0.30 | +0.12 | +0.30 | %FS |
| Gain Error | I | -7 | | +7 | %FS |
| Differential Nonlinearity (DNL) | V | | ± 0.7 | | LSB |
| Integral Nonlinearity (INL) | V | | ± 4 | | LSB |
| TEMPERATURE DRIFT | | | | | |
| Offset Error | V | | 13 | | ppm/ $^\circ\text{C}$ |
| Gain Error | V | | 200 | | ppm/ $^\circ\text{C}$ |
| POWER SUPPLY REJECTION (PSRR) | V | | 60 | | dB |
| ANALOG INPUTS (A_{IN} , \bar{A}_{IN}) ¹ | | | | | |
| Differential Input Voltage Range | V | | 2.15 | | V p-p |
| Differential Input Resistance | V | | 50 | | Ω |
| Differential Input Capacitance | V | | 2.5 | | nF |
| Input Bandwidth | IV | 0.40 | | 210 | MHz |
| VSWR ² | V | | 1.04:1 | | Ratio |
| POWER SUPPLY ³ | | | | | |
| Supply Current | | | | | |
| $I_{AV_{CC}}$ ($AV_{CC} = 5.0\text{ V}$) | I | | 0.95 | 1.05 | A |
| $I_{EV_{CC}}$ ($EV_{CC} = 3.3\text{ V}$) | I | | 0.15 | 0.2 | A |
| $I_{V_{DD}}$ ($V_{DD} = 3.3\text{ V}$) | I | | 0.49 | 0.625 | A |
| Total Power Dissipation ⁴ | I | | 6.86 | 7.5 | W |

¹ Measurement includes the recommended interface connector.

² Input VSWR, see Figure 12.

³ Supply voltages should remain stable within 65% for normal operation. However, rated ac (harmonics) performance is valid only over the range $AV_{CC} = 5.0\text{ V}$ to 5.25 V .

⁴ Power dissipation measured with encode at rated speed and -1 dBFS analog input at 10 MHz .

AD10677

DIGITAL SPECIFICATIONS

Table 2. $V_{CC} = 5\text{ V}$, $E_{VCC} = 3.3\text{ V}$, $V_{DD} = 3.3\text{ V}$; $T_A = 25^\circ\text{C}$, Differential Encode = 65 MSPS, $C_{LOAD} \leq 10\text{ pF}$, unless otherwise noted.

| Parameter | Test Level | Min | Typ | Max | Unit |
|--|------------|-----|---------------------|-----|----------|
| ENCODE INPUTS (ENCODE, ENCODEE) | | | | | |
| Differential Input Voltage Range | IV | 0.4 | | | V p-p |
| Differential Input Resistance | V | | 100 | | Ω |
| Differential Input Capacitance | V | | 160 | | pF |
| LOGIC OUTPUTS (D15 to D0) | | | | | |
| Logic Compatibility | | | CMOS | | |
| Logic 1 Voltage— $I_{LOAD} \leq 100\text{ mA}$ | IV | | $0.9 \times V_{DD}$ | | V |
| Logic 0 Voltage— $I_{LOAD} \leq 100\text{ mA}$ | IV | | 0.4 | | V |
| Output Coding | | | True Binary | | |
| Series Output Resistance—per Bit | | | 120 | | Ω |

AC SPECIFICATIONS

Table 3. $V_{CC} = 5\text{ V}$, $E_{VCC} = 3.3\text{ V}$, $V_{DD} = 3.3\text{ V}$; $T_A = 25^\circ\text{C}$, Differential Encode = 65 MSPS, $C_{LOAD} \leq 10\text{ pF}$, unless otherwise noted.

| Parameter | Test Level | Min | Typ | Max | Unit |
|--------------------------|------------|-----|------|------|------|
| SNR ¹ | | | | | |
| Analog Input | 2.5 MHz | I | 77.5 | 80 | dBFS |
| @ -1 dBFS | 10 MHz | I | 77.5 | 80 | dBFS |
| | 30 MHz | I | 76.5 | 78.5 | dBFS |
| SINAD ² | | | | | |
| Analog Input | 2.5 MHz | I | 77.2 | 79 | dBFS |
| @ -1 dBFS | 10 MHz | I | 77.2 | 79 | dBFS |
| | 30 MHz | I | 74.5 | 77 | dBFS |
| SFDR ³ | | | | | |
| Analog Input | 2.5 MHz | I | 84 | 92 | dBFS |
| @ -1 dBFS | 10 MHz | I | 84 | 92 | dBFS |
| | 30 MHz | I | 79.5 | 84 | dBFS |
| TWO-TONE ⁴ | | | | | |
| Analog Input | | | | | |
| @ -7 dBFS—IMD | | | | | |
| f1 = 10 MHz, f2 = 12 MHz | V | | 96 | | dBFS |

¹Analog input signal power at -1 dBFS; signal-to-noise (SNR) is the ratio of signal level to total noise (first five harmonics removed). Encode = 65 MSPS. SNR is reported in dBFS, related back to converter full scale.

²Analog input signal power at -1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 65 MSPS. SINAD is reported in dBFS, related back to converter full scale.

³Analog input signal at -1 dBFS; SFDR is ratio of converter full scale to worst spur.

⁴Both input tones at -7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third-order intermodulation product.

SWITCHING SPECIFICATIONS

Table 4. $AV_{CC} = 5\text{ V}$, $EV_{CC} = 3.3\text{ V}$, $V_{DD} = 3.3\text{ V}$; $T_A = 25^\circ\text{C}$, Differential Encode = 65 MSPS, $C_{LOAD} \leq 10\text{ pF}$, unless otherwise noted.

| Parameter | Test Level | Min | Typ | Max | Unit |
|---|------------|-----|------|-----|--------|
| MAXIMUM CONVERSION RATE | I | 65 | | | MSPS |
| MINIMUM CONVERSION RATE | IV | | | 15 | MSPS |
| DUTY CYCLE | IV | 40 | | 60 | % |
| ENCODE INPUT PARAMETERS | | | | | |
| Encode Period @ 65 MSPS, t_{ENC} | V | | 15.4 | | ns |
| Encode Pulse Width High @ 65 MSPS, t_{ENCH} | V | | 7.7 | | ns |
| Encode Pulse Width Low @ 65 MSPS, t_{ENCL} | V | | 7.7 | | ns |
| ENCODE/DATA (D15:0) | | | | | |
| Propagation Delay, t_{PDH} | | | 6.7 | | ns |
| Valid Time, t_{PDL} | | | 7.3 | | ns |
| APERTURE DELAY, t_A | V | | 480 | | ps |
| APERTURE UNCERTAINTY (JITTER), t_J | V | | 500 | | fs rms |
| PIPELINE DELAYS | V | | 9 | | Cycles |

EXPLANATION OF TEST LEVELS

- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C ; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. AD10677 Stress Ratings

| Parameter | Rating |
|---------------------------------------|---------------------------|
| AV _{CC} to AGND | 0 V to 7 V |
| EV _{CC} to AGND | 0 V to 6 V |
| V _{DD} to DGND | -0.5 V to +3.8 V |
| Analog Input Voltage | 0 V to AV _{CC} |
| Analog Input Current | 25 mA |
| Encode Input Voltage | 0 V to 5 V |
| Digital Output Voltage | -0.5 V to V _{DD} |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range Ambient | -65°C to +150°C |
| Maximum Operating Temperature Ambient | 92°C |

OPERATING RANGE

Operating Ambient Temperature Range: 0 C to 70 C. See the Thermal Considerations section.

Table 6. Output Coding (True Binary)

| Code | AIN (V) | Digital Output |
|-------|-----------|---------------------|
| 65535 | +1.1 | 1111 1111 1111 1111 |
| . | . | . |
| . | . | . |
| . | . | . |
| 32768 | 0 | 1000 0000 0000 0000 |
| 32767 | -0.000034 | 0111 1111 1111 1111 |
| . | . | . |
| . | . | . |
| . | . | . |
| 0 | -1.1 | 0000 0000 0000 0000 |

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TEST CIRCUITS

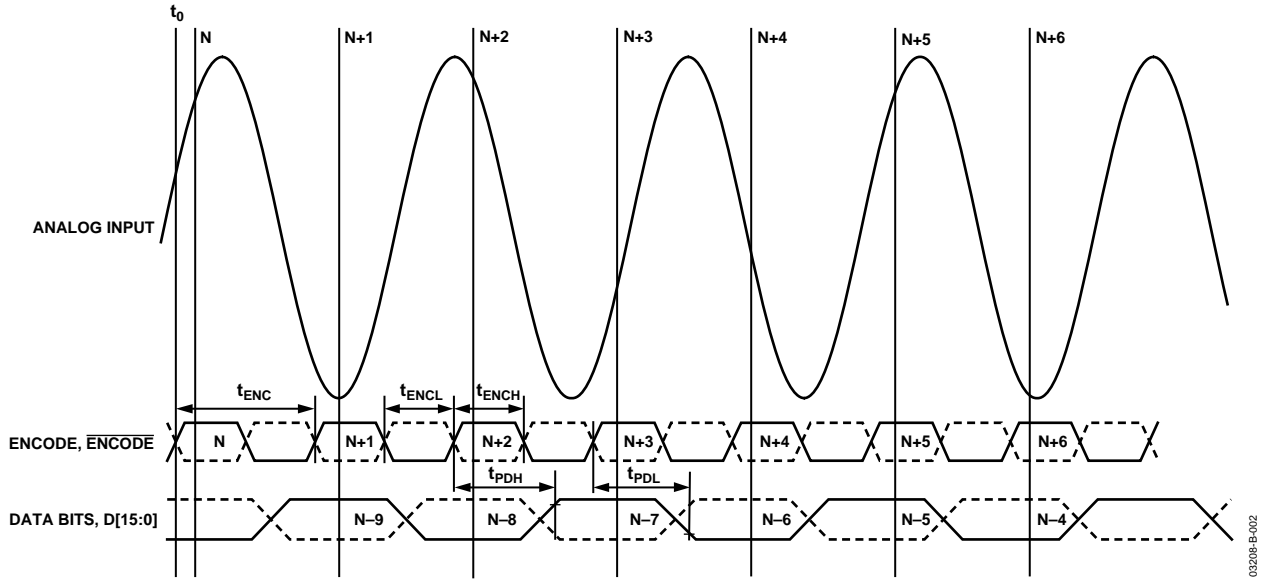


Figure 2. Timing Diagram

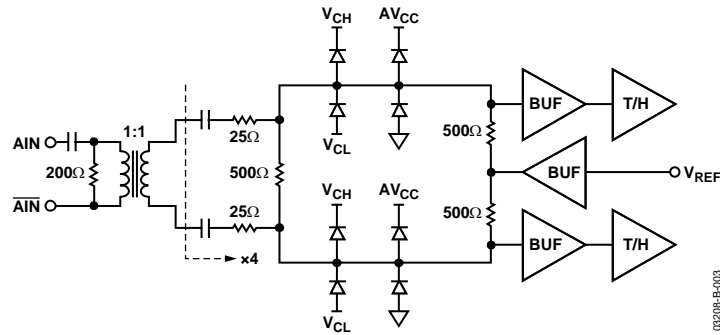


Figure 3. Analog Input Stage

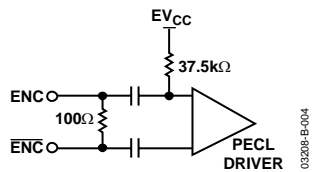


Figure 4. Equivalent Encode Input

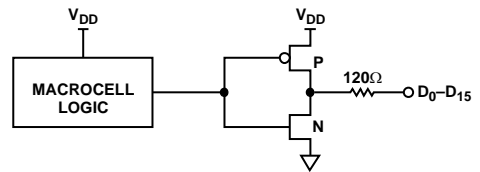


Figure 5. Digital Output Stage

AD10677

Table 7. Interfaces 1 and 2: Digital Pin Function Descriptions

| P1: Pin No. | Mnemonic | Function | P2: Pin No. | Mnemonic | Function |
|-------------|---------------------|-----------------|-------------|--------------------|------------------------------------|
| 1 | DGND | Digital Ground | 1 | DGND | Digital Ground |
| 2 | DGND | Digital Ground | 2 | DGND | Digital Ground |
| 3 | D _{OUT} 15 | Data Bit Output | 3 | +3.3VD | Digital Voltage (V _{DD}) |
| 4 | NC | No Connection | 4 | D _{OUT} 0 | Data Bit Output |
| 5 | D _{OUT} 14 | Data Bit Output | 5 | +3.3VD | Digital Voltage (V _{DD}) |
| 6 | DGND | Digital Ground | 6 | D _{OUT} 1 | Data Bit Output |
| 7 | D _{OUT} 13 | Data Bit Output | 7 | +3.3VD | Digital Voltage (V _{DD}) |
| 8 | NC | No Connection | 8 | D _{OUT} 2 | Data Bit Output |
| 9 | D _{OUT} 12 | Data Bit Output | 9 | DGND | Digital Ground |
| 10 | DGND | Digital Ground | 10 | D _{OUT} 3 | Data Bit Output |
| 11 | D _{OUT} 11 | Data Bit Output | 11 | DGND | Digital Ground |
| 12 | NC | No Connection | 12 | D _{OUT} 4 | Data Bit Output |
| 13 | D _{OUT} 10 | Data Bit Output | 13 | DGND | Digital Ground |
| 14 | DGND | Digital Ground | 14 | D _{OUT} 5 | Data Bit Output |
| 15 | D _{OUT} 9 | Data Bit Output | 15 | DGND | Digital Ground |
| 16 | NC | No Connection | 16 | D _{OUT} 6 | Data Bit Output |
| 17 | D _{OUT} 8 | Data Bit Output | 17 | +3.3VD | Digital Voltage (V _{DD}) |
| 18 | DGND | Digital Ground | 18 | D _{OUT} 7 | Data Bit Output |
| 19 | DGND | Digital Ground | 19 | +3.3VD | Digital Voltage (V _{DD}) |
| 20 | NC | No Connection | 20 | DGND | Digital Ground |

Table 8. Interface 3: Analog Pin Function Descriptions

| P3: Pin No. | Mnemonic | Function |
|-------------|-----------------|------------------------------------|
| 1 | +3.3VE | Encode Voltage (EV _{cc}) |
| 2 | +5.0VA | Analog Voltage (AV _{cc}) |
| 3 | +3.3VE | Encode Voltage (EV _{cc}) |
| 4 | +5.0VA | Analog Voltage (AV _{cc}) |
| 5 | AGND | Analog Ground |
| 6 | +5.0VA | Analog Voltage (AV _{cc}) |
| 7 | AGND | Analog Ground |
| 8 | +5.0VA | Analog Voltage (AV _{cc}) |
| 9 | AGND | Analog Ground |
| 10 | AGND | Analog Ground |
| 11 | AGND | Analog Ground |
| 12 | A _{IN} | Analog Input |
| 13 | AGND | Analog Ground |
| 14 | A _{IN} | Analog Input |
| 15 | ENCODE | Encode Input |
| 16 | AGND | Analog Ground |
| 17 | ENCODE | Encode Input |
| 18 | AGND | Analog Ground |
| 19 | AGND | Analog Ground |
| 20 | AGND | Analog Ground |

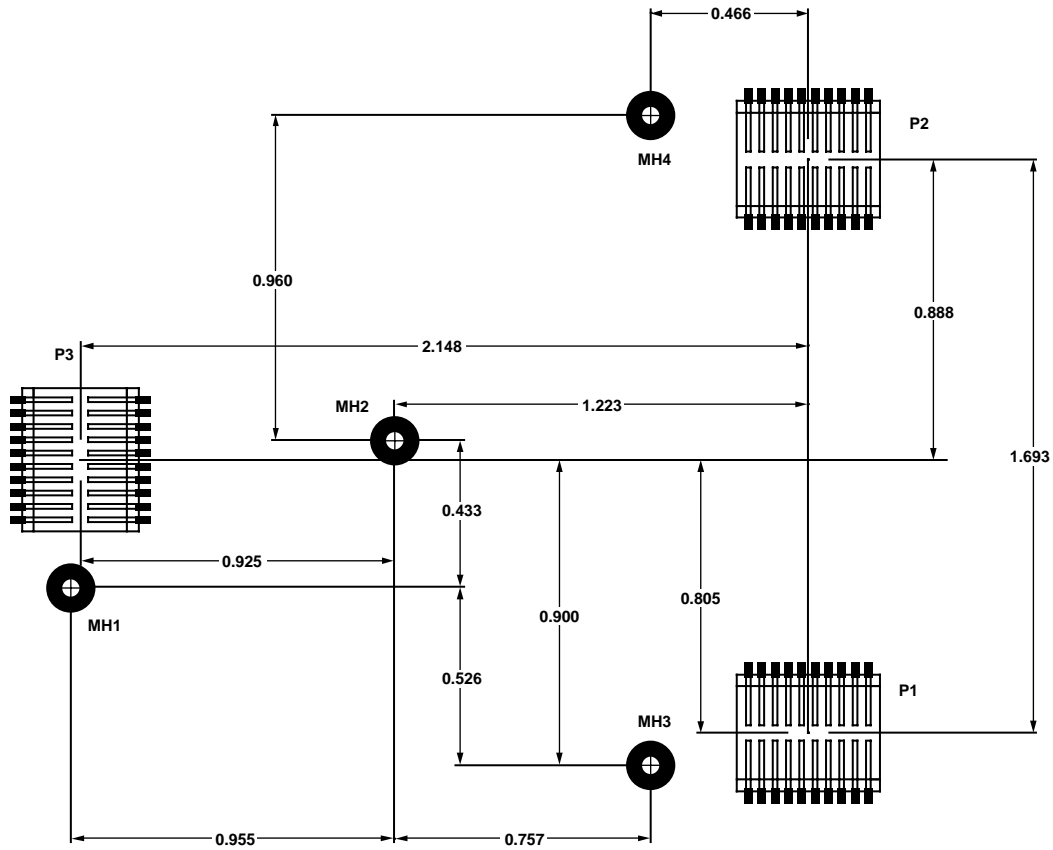
Top View of Interface PCB Assembly

Dimensions shown in inches

Tolerances:

0.xx = ±10 mils

0.xx = ±5 mils



INTERFACE NOTES

SUGGESTED INTERFACE MANUFACTURER: SAMTEC

INTERFACE PART NUMBERS FOR P1-P3: FSI-110-03-G-D-AD-K-TR (20-PIN)

HOLES 1-4 ACCOMMODATE 2-56 THREADED HARDWARE. USE FOUR 2-56 NUTS FOR SECURING THE PART TO INTERFACE PCB.

MANUFACTURER: BUILDING FASTENERS

PART NUMBER: HNSS256

DIGIKEY #: H723-ND

0320P-B-006

Figure 6. Header Interface Dimensions (Inches)

TYPICAL PERFORMANCE CHARACTERISTICS

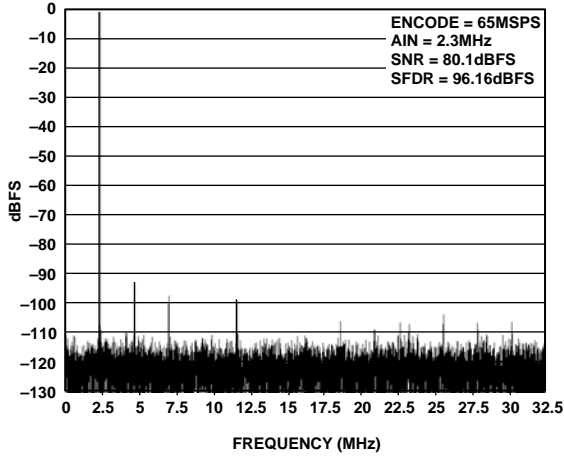


Figure 7. Single-Tone at 2.5 MHz

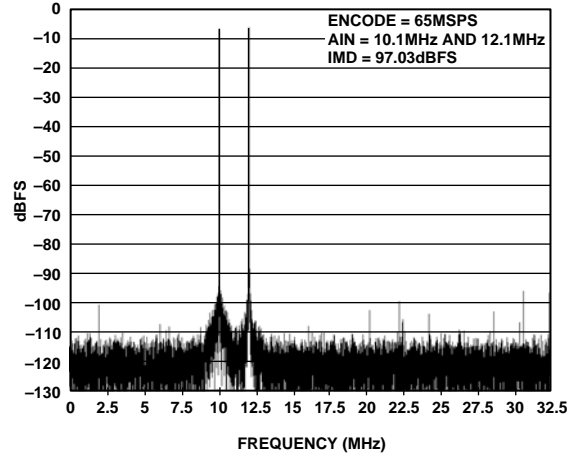


Figure 10. Two-Tone @ 10.1 MHz and 12.3 MHz

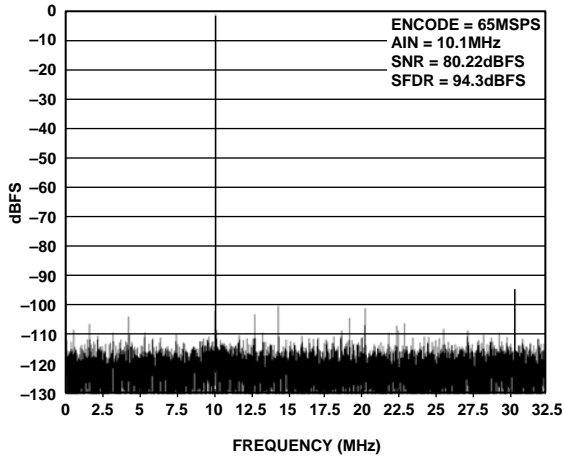


Figure 8. Single-Tone at 10 MHz

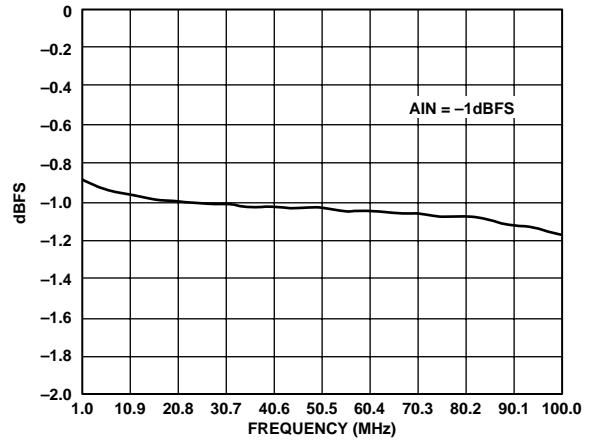


Figure 11. Gain Flatness

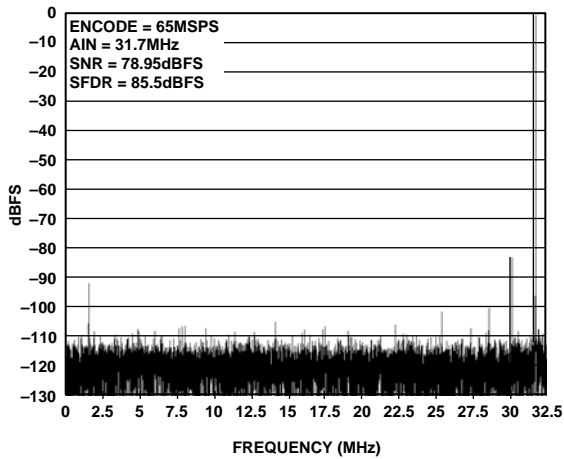


Figure 9. Single-Tone at 32 MHz

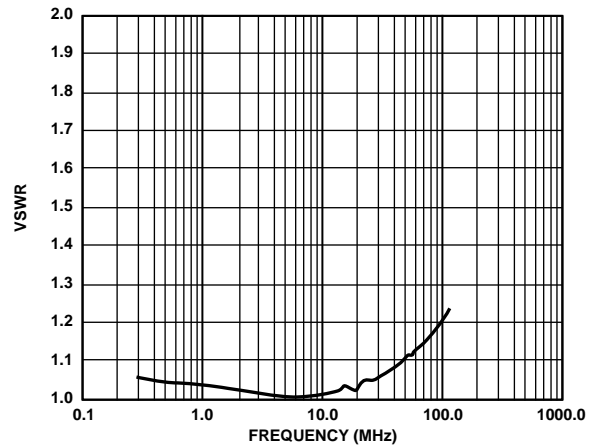


Figure 12. Analog Input VSWR

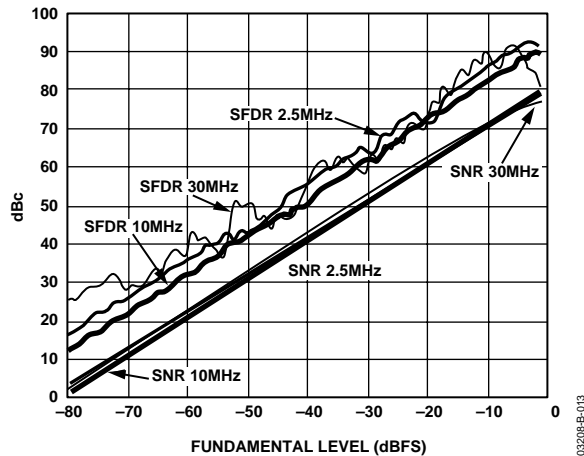


Figure 13. SFDR and SNR vs. Analog Input Level

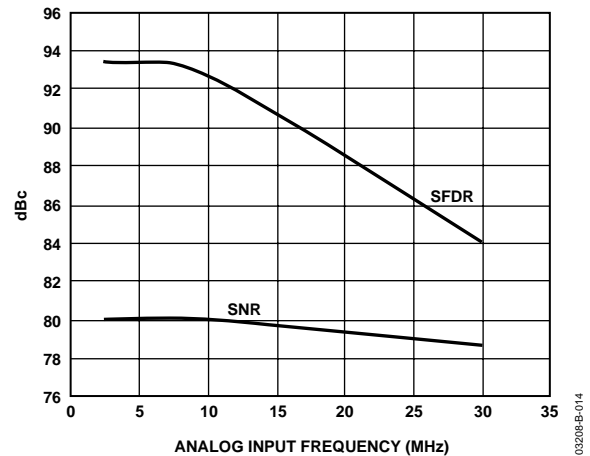


Figure 14. SFDR and SNR vs. Analog Input Frequency

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point on the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Differential Nonlinearity

The deviation of any code from an ideal 1 LSB step.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

Encode Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time the ENCODE pulse should be left in a Logic 1 state to achieve rated performance; pulse width low is the minimum time the ENCODE pulse should be left in a low state. At a given clock rate, these specifications define an acceptable encode duty cycle.

Harmonic Distortion

The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Minimum Conversion Rate

The encode rate when the SNR of the lowest analog signal frequency drops by 3 dB or less below the guaranteed limit.

Maximum Conversion Rate

The encode rate at which parametric testing is performed.

Output Propagation Delay

The delay between the 50% point of the rising edge of the ENCODE command and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio

The ratio of a change in output offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including the first five harmonics and dc. May be reported in dBc (i.e., degrades as signal levels is lowered) or in dBFS (always related back to converter full scale).

Signal-to-Noise Ratio (SNR)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc. May be reported in dBc (i.e., degrades as the signal level is lowered) or in dBFS (always related back to converter full scale).

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. SFDR may be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection (IMD)

The ratio of the rms value of an input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

Voltage Standing-Wave Ratio (VSWR)

The ratio of the amplitude of the electric field at a voltage maximum to that at an adjacent voltage minimum.

THERMAL CONSIDERATIONS

Due to the high power nature of the part, it is critical that the following thermal conditions be met for the part to perform to data sheet specifications. This also ensures that the maximum junction temperature (150°C) is not exceeded.

- Operation temperature (T_A) must be within 0° to 70°C.
- All mounting standoffs should be fastened to the interface PCB assembly with 2-56 nuts. This ensures good thermal paths as well as excellent ground points.
- The unit rises to ~72°C (T_C) on the heat sink in still air (0 linear feet per minute (LFM)). The minimum recommended air flow is 100 linear feet per minute (LFM) in either direction across the heat sink is (see Figure 15).

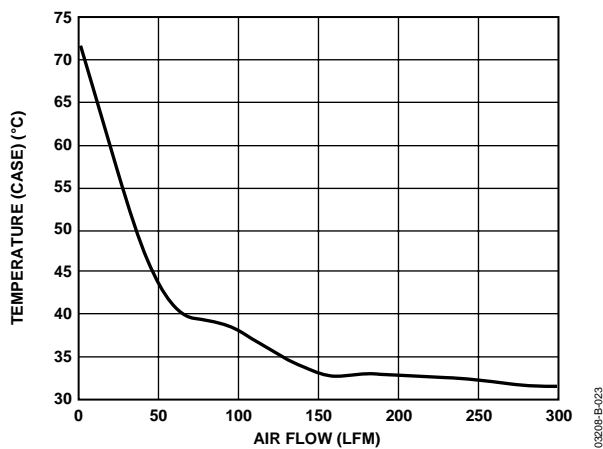


Figure 15. Temperature (Case) vs. Air Flow (Ambient)

THEORY OF OPERATION

The AD10677 uses four parallel high speed analog-to-digital converters in a correlation technique to improve the dynamic range of the ADCs. The technique sums the parallel outputs of the four converters to reduce the uncorrelated noise introduced by the individual converters. Signals processed through the high speed adder are correlated and summed coherently. Noise is not correlated and sums on an rms basis.

The four high speed analog-to-digital converters employ 3-three-stage subrange architecture. The AD10677 provides complementary analog input pins, A_{IN} and $\overline{A_{IN}}$. Each analog input is centered around 2.4 V and should swing ± 0.55 V around the reference. Since A_{IN} and $\overline{A_{IN}}$ are 180 degrees out of phase, the differential analog input signal is 2.15 V p-p.

The analog input meets a 50 Ω input impedance for easy interface to commercial cables, filters, and drivers, etc.

The AD10677 encode inputs are ac-coupled to a PECL differential receiver/driver. The output of the receiver/driver provides a clock source for a 1:5 PECL clock driver and a PECL-to-TTL translator. The 1:5 PECL clock driver provides the differential encode signal for each of the four 4 high speed

analog-to-digital converters. The PECL-to-TTL translator is used to provide a clock source for the complex programmable logic device (CPLD).

The digital outputs from the 4 ADCs drive 120 Ω series output terminators and are applied to the CPLD for postprocessing. The digital outputs are added together in the complex programmable logic device through a ripple-carry adder, which provides the 16-bit data output. The AD10677 provides valid data following nine pipeline delays. The result is a 16-bit parallel digital CMOS compatible word coded as true binary.

Input Stage

The user is provided with a single-to-differential transformer coupled input. The input impedance is 50 Ω and requires a 2.15 V p-p input level to achieve full scale.

Encoding the AD10677

The AD10677 encode signal must be a high quality, low phase noise source to prevent performance degradation. The clock input must be treated as an analog input signal because aperture jitter may affect dynamic performance. For optimum performance, the AD10677 must be clocked differentially.

Output Loading

Take care when designing the data receivers for the AD10677. The complex programmable logic device's 16-bit outputs drive 120 Ω series resistors to limit the amount of current that can flow into the output stage. To minimize capacitive loading, there should only be one gate on each of the output pins. A typical CMOS gate combined with the PCB trace has a load of approximately 10 pF. It should be noted that extra capacitive loading increases output timing and invalidates timing specifications. Digital output timing is guaranteed with 10 pF.

Analog and Digital Power Supplies

Care must be taken when selecting a power source. Linear supplies are recommended. Switching supplies tend to have radiated components that may be coupled into the ADCs. The AD10677 features separate analog and digital supply and ground currents, helping to minimize digital corruption of sensitive analog signals.

The +3.3VE supply provides power to the clock distribution circuit. The +3.3VD supply provides power to the digital output section of the ADCs, the PECL-to-TTL translator, and the CPLD. Separate +3.3VE and +3.3VD supplies are used to prevent modulation of the clock signal with digital noise. The +5VA supply provides power to the analog sections of the ADCs. Decoupling capacitors are strategically placed throughout the circuit to provide low impedance noise shunts to ground. The +5VA supply (analog power) should be decoupled to AGND (analog ground) and +3.3VD (digital power) should be decoupled to DGND (digital ground). The +3.3VE supply (analog power) should be decoupled to AGND. The evaluation board schematic and layout data show a PCB implementation of the AD10677.

ANALOG AND DIGITAL GROUNDING

While the AD10677 provides separate analog and digital ground pins, the device should be treated as an analog component. Proper grounding is essential in high speed, high resolution systems. Multilayer printed circuit boards are recommended to provide optimal grounding and power distribution. The use of power and ground planes provides distinct advantages. Power and ground planes minimize the loop area encompassed by a signal and its return path, minimize the impedance associated with power and ground paths, and provide a distributed capacitor formed by the power plane, printed circuit board material, and ground plane. The AD10677 unit has four metal standoffs (see Figure 6). MH2 is located in the center of the unit and MH1 is located directly below analog header P3. Both of these standoffs are tied to analog ground and should be connected accordingly on the next level assembly for best performance. The two standoffs located near P1 and P2 (MH3 and MH4) are tied to digital ground and should be connected accordingly on the next level assembly.

Other Notes

The circuit is configured on a 2.2" × 2.8" laminate board with three sets of connector interface pads. The pads are configured in such a way that easy keying is provided to the user. The pads are made for low profile applications and have a total height of 0.12" after mating. The part numbers for the header mates are provided in Figure 6. All pins of the analog and digital sections are described in Table 7 and Table 8.

Evaluation Board

The AD10677 evaluation board provides an easy way to test the 16-bit 65 MSPS A/D converter. The board requires a clock source, an analog input signal, two 3.3 V power supplies, and a 5 V power supply. The clock source is buffered on the board to provide the clock for the AD10677, a latch, and a data ready signal. The ADC digital outputs are latched on-board by a 74LCX16374. The digital outputs and output clock are available on a 40-pin connector J1. Power is supplied to the board via uninsulated metal banana jacks.

The analog input is connected via an SMA connector, AIN. The analog input section provides for a single-ended input option or a differential input option. The board is shipped in a single-ended analog input option. Removing a ground tie at E17 converts the circuit to a differential analog input configuration.

Table 9. PCB Bill of Material

| Item | Quantity | Reference Designator | Description |
|------|----------|---|---|
| 1 | 1 | J1 | Connector, 40-Position Header, Male Straight |
| 2 | 1 | U1 | IC, LV 16-Bit D-Type Flip-Flop with 5 V Tolerant IO |
| 3 | 3 | L1 to L3 | Common-Mode Surface-Mount Ferrite Bead 20 Ω |
| 4 | 3 | J11 to J13 | Connector, 1 mm Single Element Interface |
| 5 | 6 | P1, P2, P8 to P10, P12 | Uninsulated Banana Jack All Metal |
| 6 | 2 | U5, U6 | IC, 3.3 V/5 V ECL Differential Receiver/Driver |
| 7 | 1 | U7 | IC, 3.3 V Dual Differential LVPECL to LVTTTL Translator |
| 8 | 1 | R24 | RES 0.0 Ω 1/10 W 5% 0805 SMD |
| 9 | 19 | R0 to R16, R20, R23 | RES 51.1 Ω 1/10 W 1% 0805 SMD |
| 10 | 1 | R17 | RES 18.2 kΩ 1/10 W 1% 0805 SMD |
| 11 | 4 | R18, R19, R21, R22 | RES 100 Ω 1/10 W 1% 0805 SMD |
| 12 | 17 | C1, C10 to C13, C16 to C18, C23 to C26, C29 to C32 | CAP 0.1 μF 16 V Ceramic X7R 0805 |
| 13 | 6 | C8, C9, C4, C15, C27, C33 | CAP 10 μF 10 V Ceramic Y5V 1206 |
| 14 | 4 | J2, J3, J5, J6 | Connector, SMA Jack 200 Mil STR Gold |
| 15 | 1 | A1 | Assembly, AD10677BWS |
| 16 | 1 | AD106xx Evaluation Board | GS04483 (PCB) |

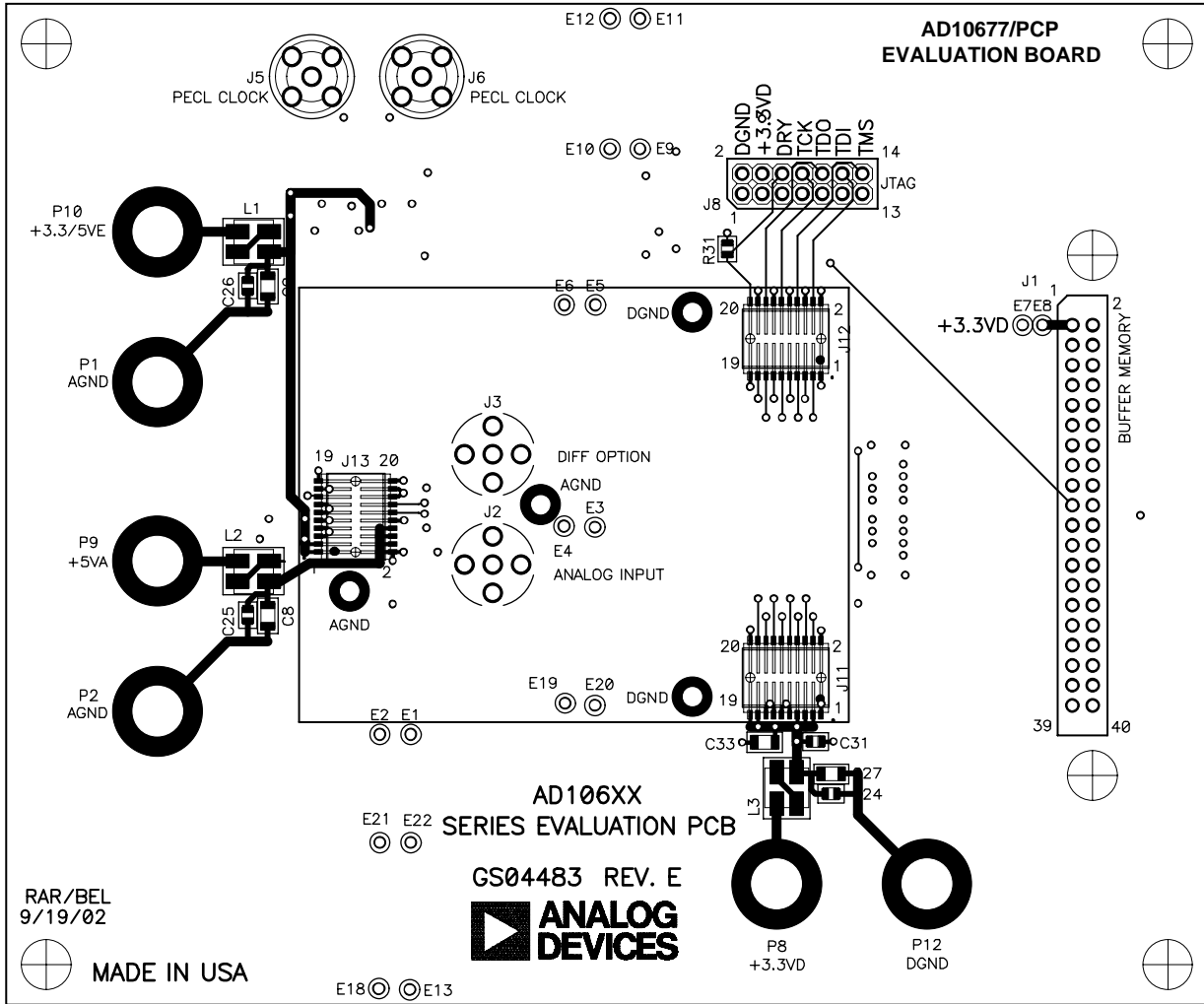
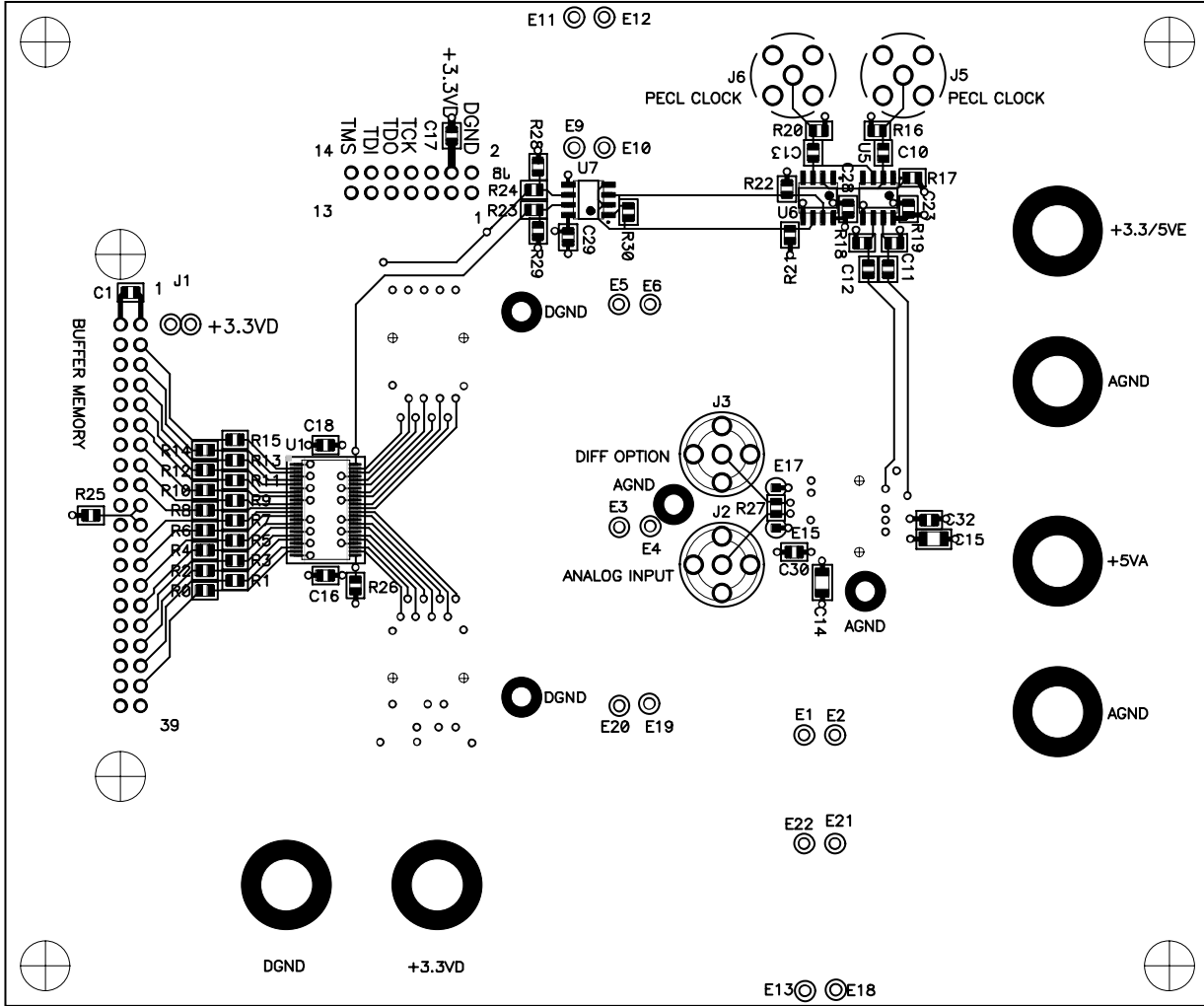


Figure 17. Evaluation Board Mechanical Layout, Top View



032308-B-018

Figure 18. Evaluation Board Mechanical Layout, Bottom View

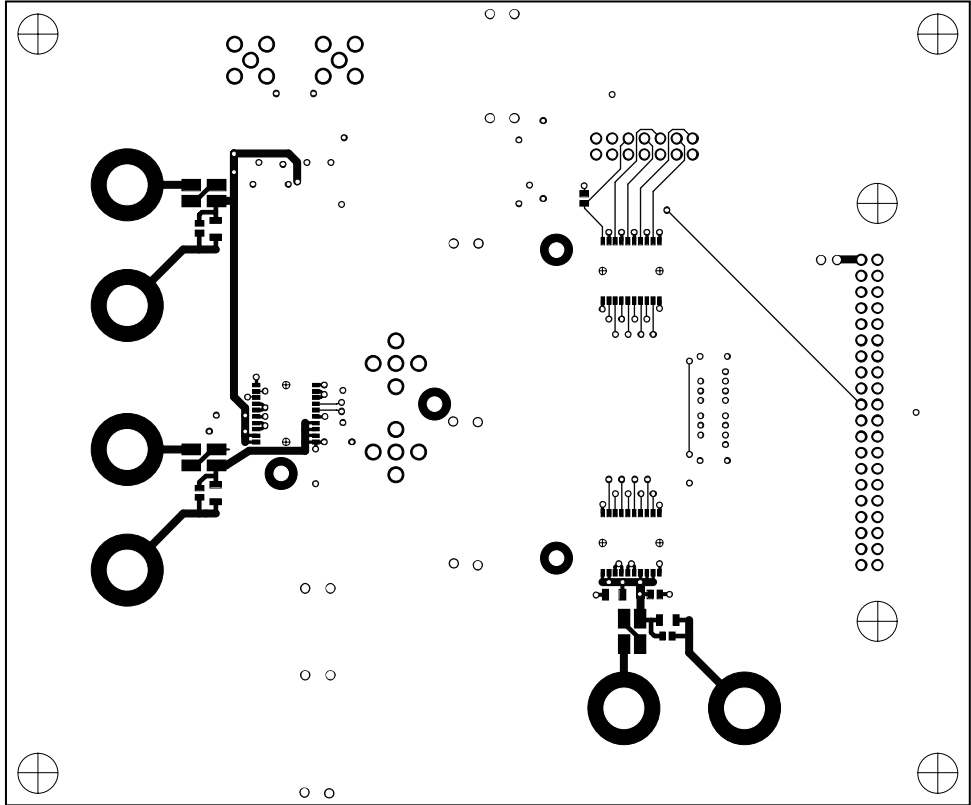


Figure 19. Evaluation Board Top Layer Copper

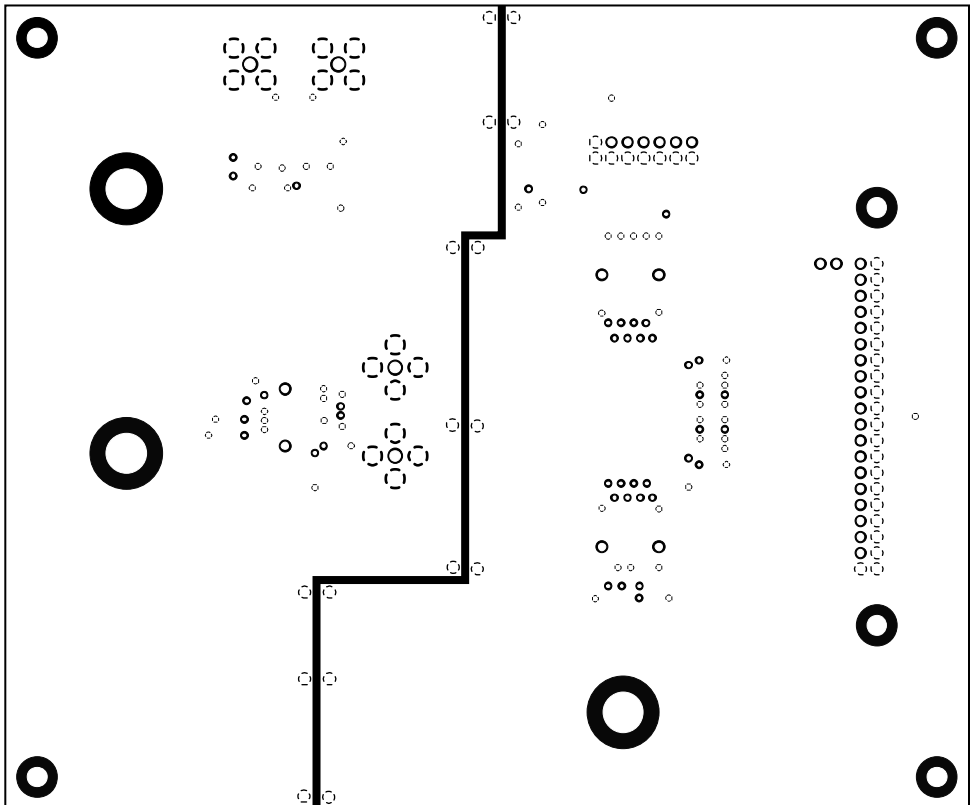
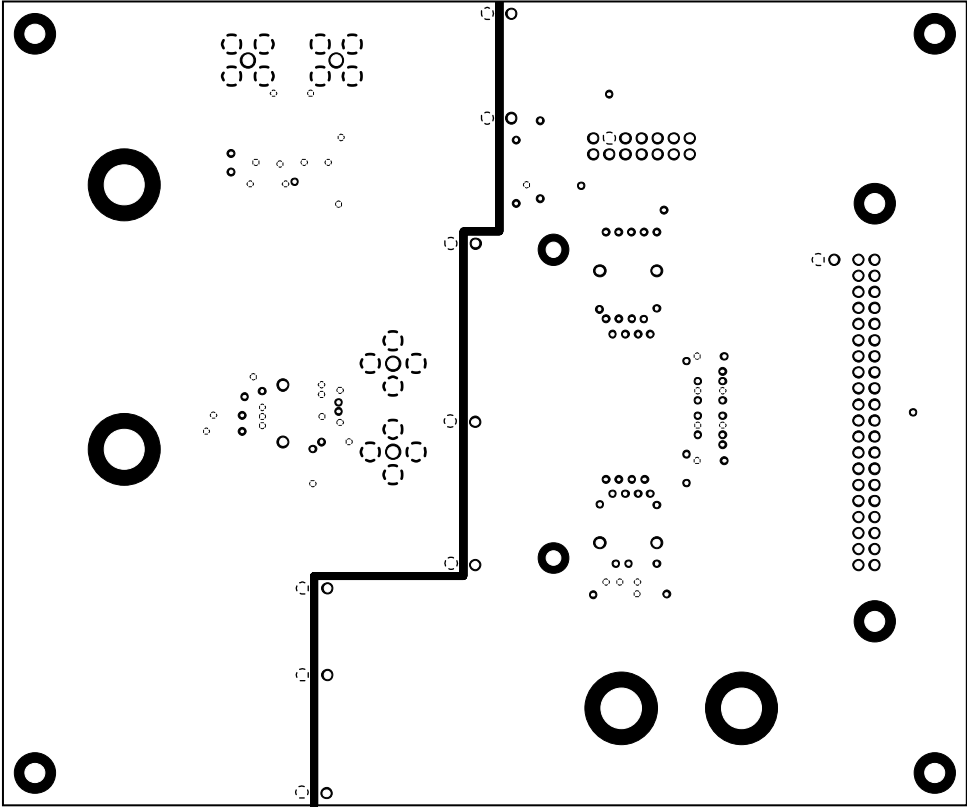
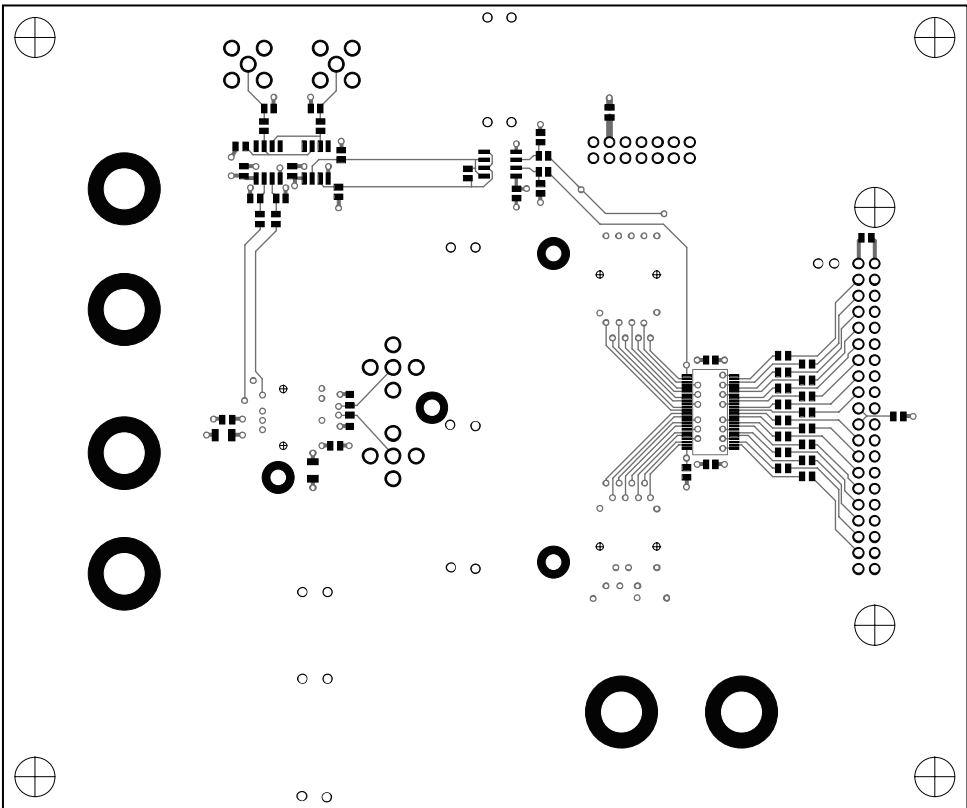


Figure 20. Evaluation Board Second Layer Copper



032108-B-021

Figure 21. Evaluation Board Third Layer Copper



032108-B-022

Figure 22. Evaluation Board Bottom Layer Copper

OUTLINE DIMENSIONS

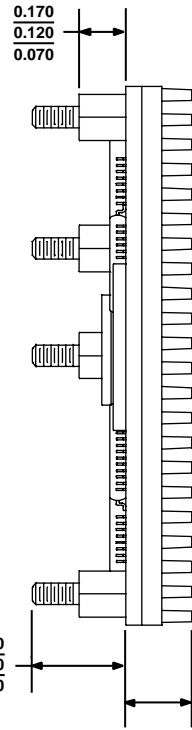
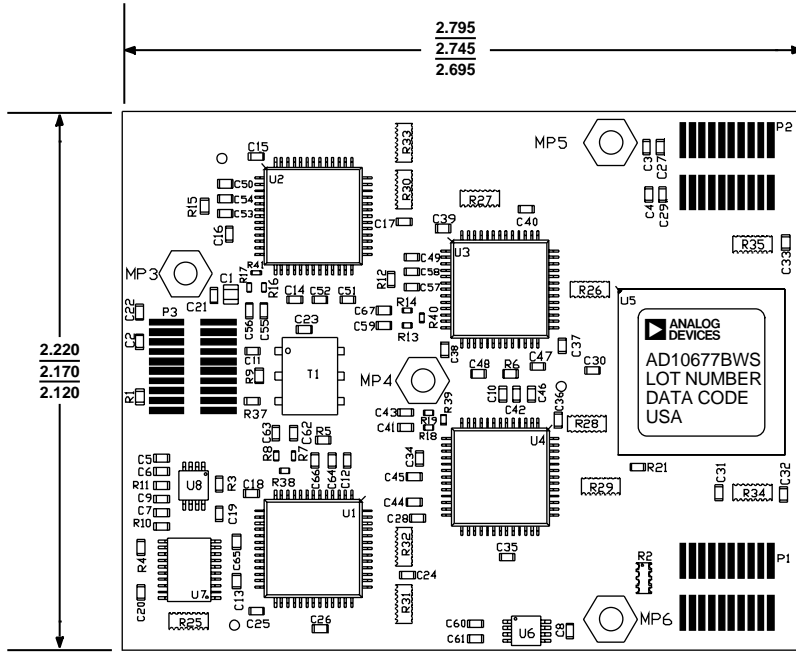
Dimensions shown in inches

Tolerances:

0.xx = ±10 mils

0.xxx = ±5 mils

Bottom View



Top View

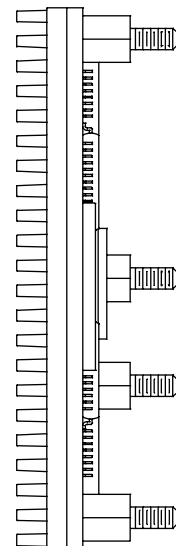
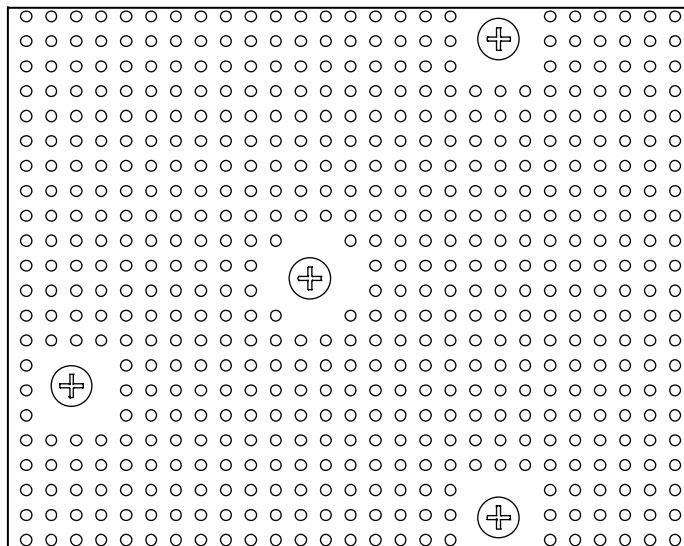


Figure 23

AD10677

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-------------|-------------------|--|----------------|
| AD10677BWS | 0°C to 70°C | Non-Herm Hybrid Surf Mount (2.2" × 2.8") | WS-120 |
| AD10677/PCB | 25°C | Evaluation Board | |