

MC44871

Advance Information

PLL Tuning Circuit with DC-DC Converter, I²C Bus and ADC

The MC44871 is a tuning circuit for TV, VCR and Multimedia tuner applications. This device contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44871 has an integrated dc/dc converter to generate the 30 V supply voltage for the tuning amplifier on the chip. A tuner using the MC44871 does not require an external 30 V supply.

The MC44871 is controlled by a I²C bus, and has a chip address function. The MC44871 data format is the same as the MC44818.

The MC44871 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- The Pin Called V_{CC2} for the MC44818 is Now Called CP (Charge Pump). This Pin is the Output of the DC/DC Converter; a 1.0 nF Capacitor Replaces the Need for an External 30 V Supply
- High Speed I²C Bus (up to 800 kHz)
- I²C Bus Read Mode for Lock Detector and AFC Level
- HF Input is Balanced
- MC44871 has Three PNP High Current (30 mA) Band Buffers (B0, B1, B2) and One NPN Low Current (5.0 mA) Band Buffer (B4)
- V_{CC} Internally Supplies PNP Band Buffers
- The Tuning Voltage is Generated Through an External Pull-Up Resistor (750 kΩ)
- Less Phase Comparator Output Current
- Single 5.0 V Supply Operation

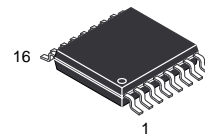
MOSAIC is a trademark of Motorola, Inc.

ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|------------|--------------------------------|----------|
| MC44871DTB | T _A = -20° to +85°C | TSSOP-16 |

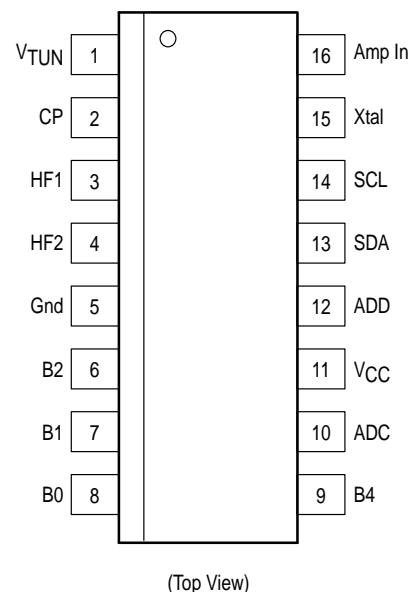
PLL TUNING CIRCUIT WITH HIGH SPEED I²C BUS AND 30 V TUNING SUPPLY

SEMICONDUCTOR TECHNICAL DATA



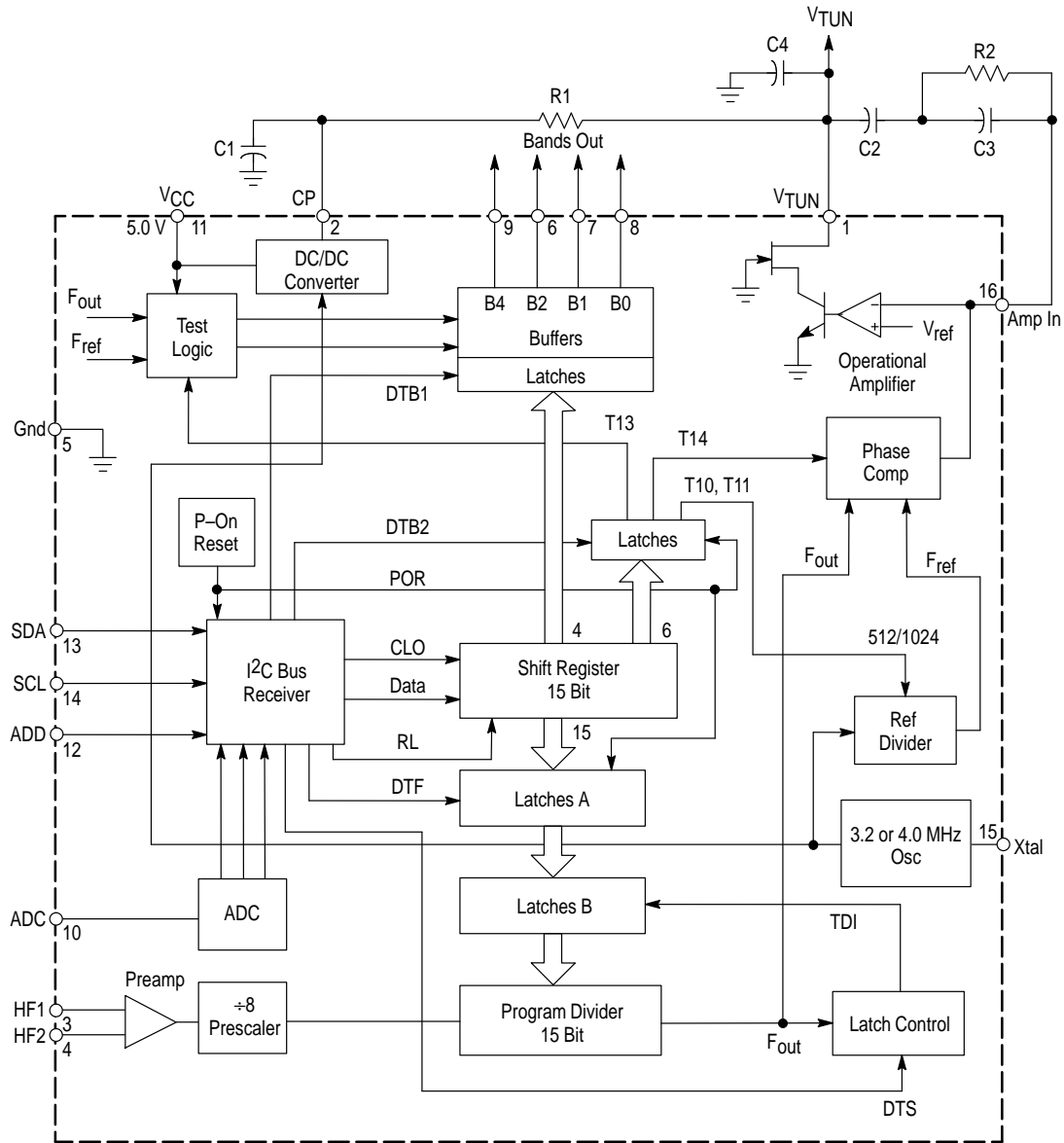
DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP-16)

PIN CONNECTIONS (16 Pin TSSOP)



MC44871

Figure 1. Representative Block Diagram



This device contains 3,204 active transistors.

Approximate values of the external components for generation of the tuning voltage are:

- | | |
|--|-----------------------------------|
| C1 = 1.0 nF | Charge Pump filter capacitor |
| R1 = 750 k Ω (560 k Ω minimum) | Pull-up resistor |
| C4 = 330 pF | V _{TUN} filter capacitor |
| C2 = 47 nF, C3 = 22 nF, R2 = 39 k Ω | Loop filter |
- These component values depend on the application.

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MAXIMUM RATINGS (Maximum ratings are those values beyond which permanent damage to the device may occur. Exposure to those limits may also affect device reliability; $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Rating | Pin | Value | Unit |
|--|---------|-------------|------------------|
| Power Supply Voltage (V_{CC}) | 11 | 6.0 | V |
| Storage Temperature | – | –65 to +150 | $^\circ\text{C}$ |
| Operating Temperature Range | – | –20 to +85 | $^\circ\text{C}$ |
| Operational Amplifier Output Voltage | 1 | 40 | V |
| RF Input Level 80 MHz to 1.3 GHz | 3, 4 | 1.5 | V _{rms} |
| NPN Band Buffer "Off" Voltage | 9 | 10 | V |
| NPN Band Buffer "On" Current | 9 | 15 | mA |
| PNP Band Buffer "Off" Voltage | 6, 7, 8 | 6.0 | V |
| PNP Band Buffer "On" Current | 6, 7, 8 | 50 | mA |
| PNP Band Buffer – Short Circuit Duration (Note 1) | 6, 7, 8 | Continuous | – |
| Band Buffer Operation at 40 mA all PNP Buffers "On" | 6, 7, 8 | 10 | s |

NOTES: 1. At $V_{CC} = 5.0\text{ V}$ and $T_A = -20^\circ$ to $+80^\circ\text{C}$ one buffer "On" only.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (Parameter Type: A–100% Tested, B–100% Correlation Tested, C–Characterized on Samples, D–Design Parameter, $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified, 750 k Ω pull-up resistor between CP [Pin2] and VTUN [Pin 1].)

| Characteristic | Pin | Min | Typ | Max | Unit | Type |
|--|---------|------|------|------|---------------|------|
| V_{CC} Supply Voltage Range | 11 | 4.5 | 5.0 | 5.5 | V | A |
| V_{CC} Supply Current (All Buffers "Off") | 11 | – | 35 | 45 | mA | A |
| One Buffer "On" when Open | | – | 40 | 50 | | B |
| One Buffer "On" at 40 mA | | – | 80 | 90 | | B |
| PNP Band Buffer B0, B1, B2 Leakage Current when "Off" | 6, 7, 8 | – | 0.01 | 1.0 | μA | A |
| PNP Band Buffer B0, B1, B2 Saturation Voltage when "On" at 30 mA | 6, 7, 8 | – | 200 | 500 | mV | B |
| NPN Band Buffer B4 Leakage Current when "Off" | 9 | – | 0.01 | 1.0 | μA | A |
| NPN Band Buffer "Off" Voltage | 9 | 0 | – | 5.5 | V | D |
| NPN Band Buffer B4 Saturation Voltage when "On" at 1.0 μA | 9 | – | 50 | 100 | mV | A |
| NPN Band Buffer B4 Voltage when "On" @ 5.0 mA | 9 | – | 1.2 | 1.6 | V | A |
| Reference Oscillator Frequency Range | 15 | 3.15 | 3.2 | 4.05 | MHz | D |
| Phase Comparator 3–State Current | 16 | –15 | 0 | 15 | nA | A |
| Phase Comparator Output Current – High Value | 16 | 12 | 20 | 28 | μA | A |
| Phase Comparator Output Current – Low Value | 16 | 2.0 | 6.0 | 10 | μA | A |
| DC–DC Converter Output Voltage, Sourcing 50 μA | 2 | 28 | 31 | 34.5 | V | A |
| DC–DC Converter Maximum Current, Output Short Circuited | 2 | – | 200 | 350 | μA | A |
| DC–DC Converter setting time from $V_{CC} > 4.5\text{ V}$ to DC–DC Converter Voltage $> 28\text{ V}$ @ Load = 750 k Ω /1.0 nF | 2 | – | – | 25 | ms | C |
| Operational Amplifier Internal Reference Voltage (V_{ref}) | – | 1.3 | 1.9 | 2.5 | V | A |
| Operational Amplifier Input Current | 16 | –15 | 0 | 15 | nA | A |
| Operational Amplifier DC Open Loop Gain | – | 100 | 300 | – | – | A |
| Operational Amplifier Gain Bandwidth Product ($C_L = 1.0\text{ nF}$) | – | 0.3 | – | – | MHz | D |
| Operational Amplifier Low Output Voltage, Sinking 50 μA | 16 | – | 0.2 | 0.4 | V | D |
| Oscillator – Negative Resistance | 15 | 1.0 | – | – | k Ω | D |

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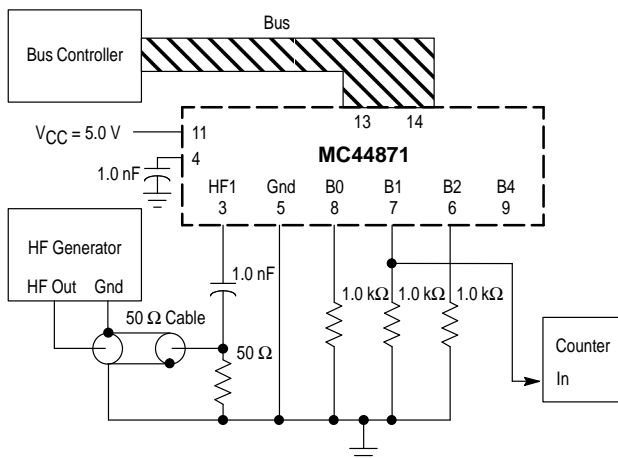
PIN FUNCTION DESCRIPTION (see Figure 1)

| Pin | Symbol | Description |
|---------|------------------|--|
| 1 | V _{TUN} | Operational amplifier output which provides the tuning voltage |
| 2 | CP | DC-DC Converter output (Charge Pump) |
| 3, 4 | HF1, HF2 | Symmetrical HF inputs |
| 5 | Gnd | Ground |
| 6, 7, 8 | B2, B1, B0 | PNP Band Buffer outputs |
| 9 | B4 | NPN Band Buffer output |
| 10 | ADC | Three bit ADC for Automatic Frequency Tuning, readable through the bus |
| 11 | V _{CC} | Positive supply of the circuit (5.0 V) |
| 12 | ADD | Chip address function |
| 13 | SDA | I ² C bus Data Input/Output |
| 14 | SCL | I ² C bus Clock |
| 15 | Xtal | Crystal Oscillator (3.2 MHz or 4.0 MHz) |
| 16 | Amp In | Operational amplifier input |

HF INPUT SENSITIVITY AND OVERLOAD CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C.) (See Figure 2.)

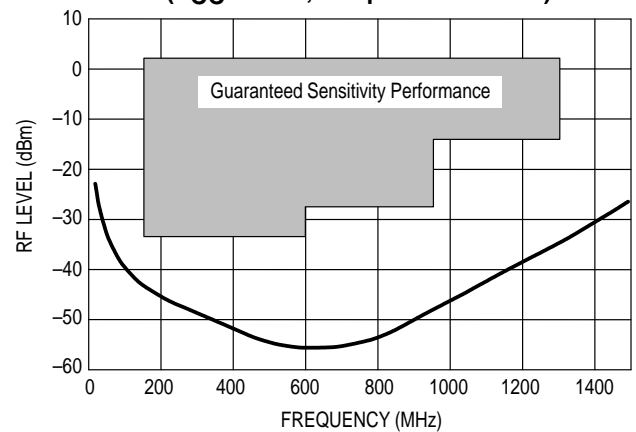
| Characteristics | Pin | Min | Typ | Max | Unit | Type |
|--------------------|------|-----|-----|-----|-------|------|
| DC Bias (Internal) | 3, 4 | – | 1.6 | – | V | A |
| 80–150 MHz | 3, 4 | 10 | – | 315 | mVrms | C |
| 150–600 MHz | 3, 4 | 5.0 | – | 315 | mVrms | C |
| 600–950 MHz | 3, 4 | 10 | – | 315 | mVrms | C |
| 950–1300 MHz | 3, 4 | 50 | – | 315 | mVrms | C |

Figure 2. HF Sensitivity Test Circuit



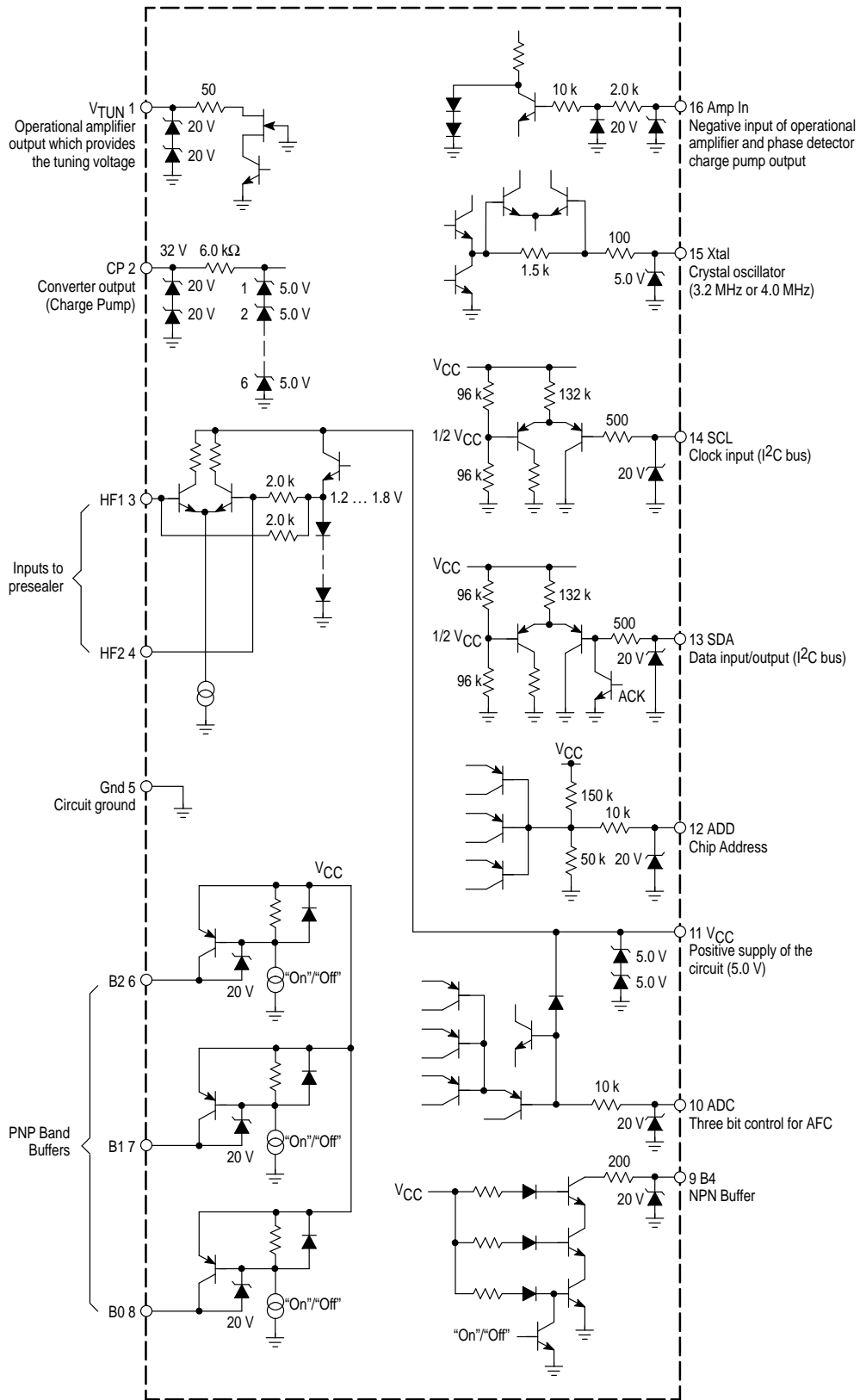
NOTE: 1. Device is in test mode. B1, B2 are "On" and B0, B4 are "Off". Sensitivity is level of HF generator on 50 Ω load.

Figure 3. Typical HF Sensitivity Performance (V_{CC} = 5.0 V, Temperature = 25°C)



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Figure 4. Pin Circuit Schematic



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HIGH SPEED I²C BUS (The circuit is controlled by a I²C bus with a Serial Data [SDA], Serial Clock [SCL], Chip Address Control [ADD] inputs. The device I²C bus has a read mode [odd addresses] and a write mode [even addresses].)

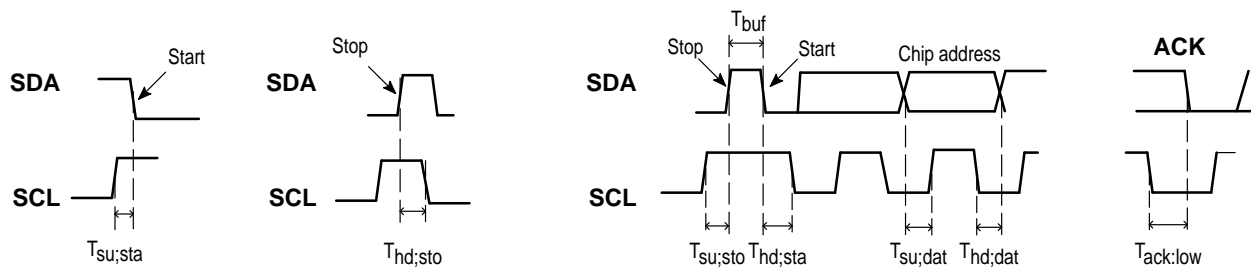
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.)

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit | Type |
|--|--------|----------|----------------|-----|----------------|---------------|------|
| SDA/SCL Output Current at 0 V | 13, 14 | | – | – | 10 | μA | A |
| SDA/SCL Low Input Level | 13, 14 | V_{IL} | – | – | 1.5 | V | B |
| SDA/SCL High Input Level | 13, 14 | V_{IH} | 3.0 | – | – | V | B |
| SDA/SCL Input Current for Input Level from 0.4 V to 0.3 V_{CC} | 13, 14 | | –5.0 | 0 | 5.0 | μA | C |
| SDA/SCL Input Level | 13, 14 | | 0 | – | $V_{CC} + 0.3$ | V | D |
| ADD Input Level | 12 | | –0.01 V_{CC} | – | 1.1 V_{CC} | | D |
| SDA/SCL Capacitance | 13, 14 | C_i | – | – | 10 | pF | C |
| SDA Low Output Level (sinking 3.0 mA) | 13 | | – | 0.3 | 1.0 | V | A |
| SDA Low Output Level (sinking 15 mA) | 13 | | – | – | 1.5 | V | C |

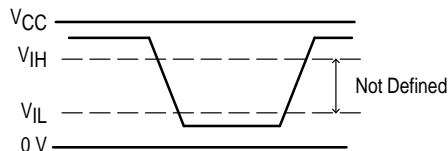
TIMING CHARACTERISTICS

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit | Type |
|--|--------|---------------|-----|-----|-----|------|------|
| Bus Clock Frequency | 14 | | 0 | – | 800 | kHz | C |
| Bus Free Time Between Stop and Start | – | T_{buf} | 200 | – | – | ns | C |
| Setup Time for Start Conditions | – | $T_{su;sta}$ | 500 | – | – | ns | C |
| Hold Time for Start Condition | – | $T_{hd;sta}$ | 500 | – | – | ns | C |
| Data Setup Time | – | $T_{su;dat}$ | 0 | – | – | ns | C |
| Data Hold Time | – | $T_{hd;dat}$ | 0 | – | – | ns | C |
| Setup Time for Stop Condition | – | $T_{su;sto}$ | 500 | – | – | ns | C |
| Hold time for Stop Condition | – | $T_{hd;sto}$ | 500 | – | – | ns | C |
| Acknowledge Propagation Delay | | $T_{ack;low}$ | – | – | 300 | ns | C |
| SDA Fall Time at 3.0 mA sink I and 130 pF Load | 13 | | – | – | 50 | ns | C |
| SDA Fall Time at 3.0 mA sink I and 400 pF Load | 13 | | – | – | 80 | ns | C |
| SDA/SCL Rise Time | 13, 14 | | – | – | 300 | ns | C |
| SCL Fall Time | 13, 14 | | – | – | 300 | ns | C |
| Pulse Width of Spikes Suppressed by the Input Filter | 13, 14 | T_{sp} | – | – | 50 | ns | C |

Timings Definition

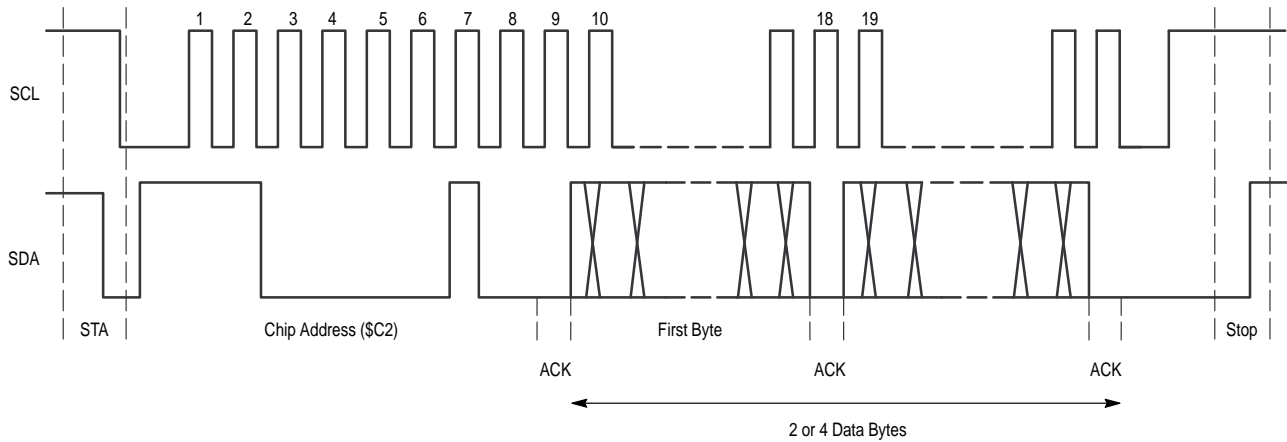


Levels Definition



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Figure 5. High Speed I²C Compatible Bus Data Format



I²C Write Mode Format and Bus Receiver

The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I²C bus receiver. The definition of the permissible bus protocol is shown below:

```

1_STA CA CO BA FM FL STO
2_STA CA FM FL CO BA STO
3_STA CA CO BA STO
4_STA CA FM FL STO
  
```

STA = Start Condition
 CA = Chip Address Byte
 CO = Control Information
 BA = Band Information
 FM = Frequency Information with MSB
 FL = Frequency Information with LSB
 STO = Stop Condition

Figure 5 shows the five bytes of information that are needed for circuit operation: the chip address, two bytes of control and information, and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received, the third one is

ignored. If five or more data bytes are received, the fifth and following ones are ignored, and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information. If the function bit is logic "1", the two following bytes contain control and band information. The first data byte, after the chip address, may be byte CO or byte FM. The two bytes of frequency information are preceded by a logic "0".

Chip Address

Even addresses are for write mode, and odd addresses are for read mode. Chip address is programmable by Pin 12 (ADD).

| ADD Pin 12 | Address (HEX.) |
|--|----------------|
| -0.01 V _{CC} to 0.1 V _{CC} | C0/C1 |
| 0.2 V _{CC} to 0.3 V _{CC} (or Open) | C2/C3 |
| 0.4 V _{CC} to 0.7 V _{CC} | C4/C5 |
| 0.8 V _{CC} to 1.1 V _{CC} | C6/C7 |

The Two Permissible Protocols with Five Bytes

| | | | | | | | | | |
|--------------------------|----|-----|-----|-----|-----|-----|-----|----|-----|
| CA_Chip Address | 1 | 1 | 0 | 0 | 0 | 0/1 | 0/1 | 0 | ACK |
| | | | | | | | | | |
| CO_Control Information | 1 | T14 | T13 | T12 | T11 | T10 | T9 | T8 | ACK |
| BA_Band Information | X | X | X | B4 | X | B2 | B1 | B0 | ACK |
| | | | | | | | | | |
| FM_Frequency Information | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | ACK |
| FL_Frequency Information | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | ACK |

| | | | | | | | | | |
|--------------------------|----|-----|-----|-----|-----|-----|-----|----|-----|
| CA_Chip Address | 1 | 1 | 0 | 0 | 0 | 0/1 | 0/1 | 0 | ACK |
| | | | | | | | | | |
| FM_Frequency Information | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | ACK |
| FL_Frequency Information | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | ACK |
| | | | | | | | | | |
| CO_Control Information | 1 | T14 | T13 | T12 | T11 | T10 | T9 | T8 | ACK |
| BA_Band Information | X | X | X | B4 | X | B2 | B1 | B0 | ACK |

I²C Read Mode Format

The incoming information consists of the chip address byte in read mode (odd address). The device then answers with an acknowledge followed by a byte containing lock and ADC information. There is no ACK pulse sent after this byte.

1_STA CA ADC_LO
 ADC_LO = ADC and Lock information

I²C Read Format

| | | | | | | | | | |
|-----------------|---|----|---|---|---|-----|-----|-----|----------|
| CA_Chip Address | 1 | 1 | 0 | 0 | 0 | 0/1 | 0/1 | 1 | ACK |
| | | | | | | | | | |
| ADC_LO | 1 | LO | X | X | X | AD2 | AD1 | AD0 | (no ACK) |

Definition of the Bits for Test and Features

Bits B0, B1, B2: Control the PNP Band Buffers

| | |
|----------------|-----------------------------|
| B0, B1, B2 = 0 | Buffer is "Off", Output Low |
| = 1 | Buffer is "On", Output High |

Bit B4: Controls the NPN Band Buffer

| | |
|--------|------------------------------|
| B4 = 0 | Buffer is "Off", Output High |
| = 1 | Buffer is "On", Output Low |

Bit T8: Controls the Operational Amplifier Output

| T8 | Operation |
|--------|---|
| T8 = 0 | Operational Amplifier Normal Operation |
| = 1 | Output State of Operational Amplifier Switched Off Output Pulls High through External Resistor |

Bit T10, T11: Control the Reference Divider

| T10 | T11 | Divider Ratio |
|-----|-----|---------------|
| 0 | 0 | 512 |
| 0 | 1 | 1024 |
| 1 | 0 | 1024 |
| 1 | 1 | 512 |

Bit T9, T12: Control the Phase Comparator

| T9 | T12 | Function |
|----|-----|-------------------|
| 0 | 0 | Upper Source Only |
| 0 | 1 | Lower Source Only |
| 1 | 0 | Normal Operation |
| 1 | 1 | High Impedance |

Bit T13: Switches the Band Buffer Output to Test Mode

| | |
|---------|--|
| T13 = 0 | Normal Operation |
| = 1 | Test Mode: F_{ref} Out at B2 F_{by2} Out at B1 |

In the test mode, B2 and B1 have to be ON (B2=B1=1). F_{ref} is the reference frequency. F_{by2} is the output frequency of the programmable divider divided-by-2.

Bit T14: Controls the Charge Pump Current

| | |
|---------|--------------------------|
| T14 = 0 | Pump Current 5.0 μ A |
| = 1 | Pump Current 20 μ A |

Bit AD2, AD1, AD0: Indicate the ADC Pin Analog Level

| ADC Input Voltage | AD2 | AD1 | AD0 |
|-----------------------|-----|-----|-----|
| 0 to 0.18 V_{CC} | 0 | 0 | 0 |
| 0.18 to 0.34 V_{CC} | 0 | 0 | 1 |
| 0.34 to 0.5 V_{CC} | 0 | 1 | 0 |
| 0.5 to 0.66 V_{CC} | 0 | 1 | 1 |
| 0.66 to 0.82 V_{CC} | 1 | 0 | 0 |
| 0.82 to 1.0 V_{CC} | 1 | 0 | 1 |

Bit LO: Indicates the Status of Lock Detector

| | |
|--------|-----------------------|
| LO = 0 | PLL Status Not Locked |
| LO = 1 | PLL Status Locked |

Figure 6. Equivalent Circuit of the Integrated PNP Band Buffers

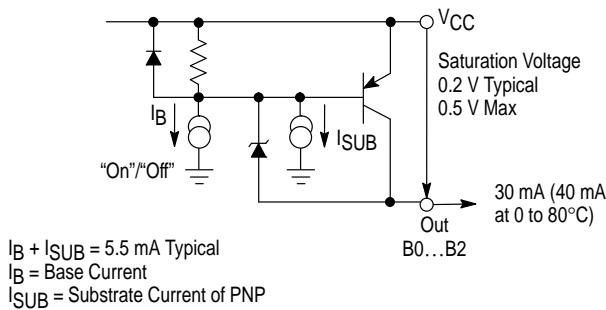
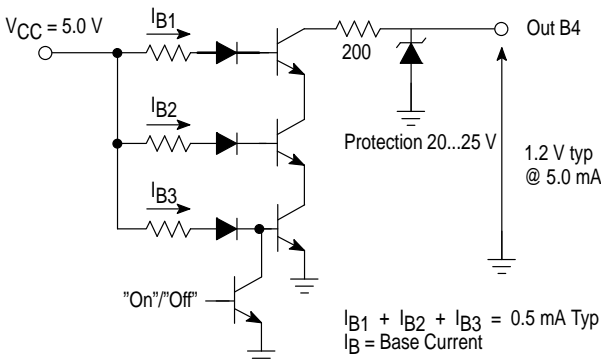


Figure 7. Equivalent Circuit of the Integrated NPN Band Buffer



OPERATING DESCRIPTION

Introduction

A representative block diagram and typical system application are shown in Figures 1 and 8. A discussion of the features and function of each of the internal blocks is given.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:
 $N = 16384 \times N_{14} + 8192 \times N_{13} + \dots + 4 \times N_2 + 2 \times N_1 + N_0$
 Maximum Ratio 32767 Minimum Ratio 256

$N_0 \dots N_{14}$ are the different bits for frequency information.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of $N = 256$ or higher.

The Prescaler

The divide-by-8 prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is both phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Operational Amplifier

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier output (Pin 1) needs an external 750 k Ω pull-up resistor (560 k Ω minimum). This minimum value is defined by the charge pump output current capability.

The Oscillator

The oscillator uses a 3.2 or a 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in the series resonance mode.

The voltage at Pin 15 has low amplitude and low harmonic distortion.

Power Dissipation

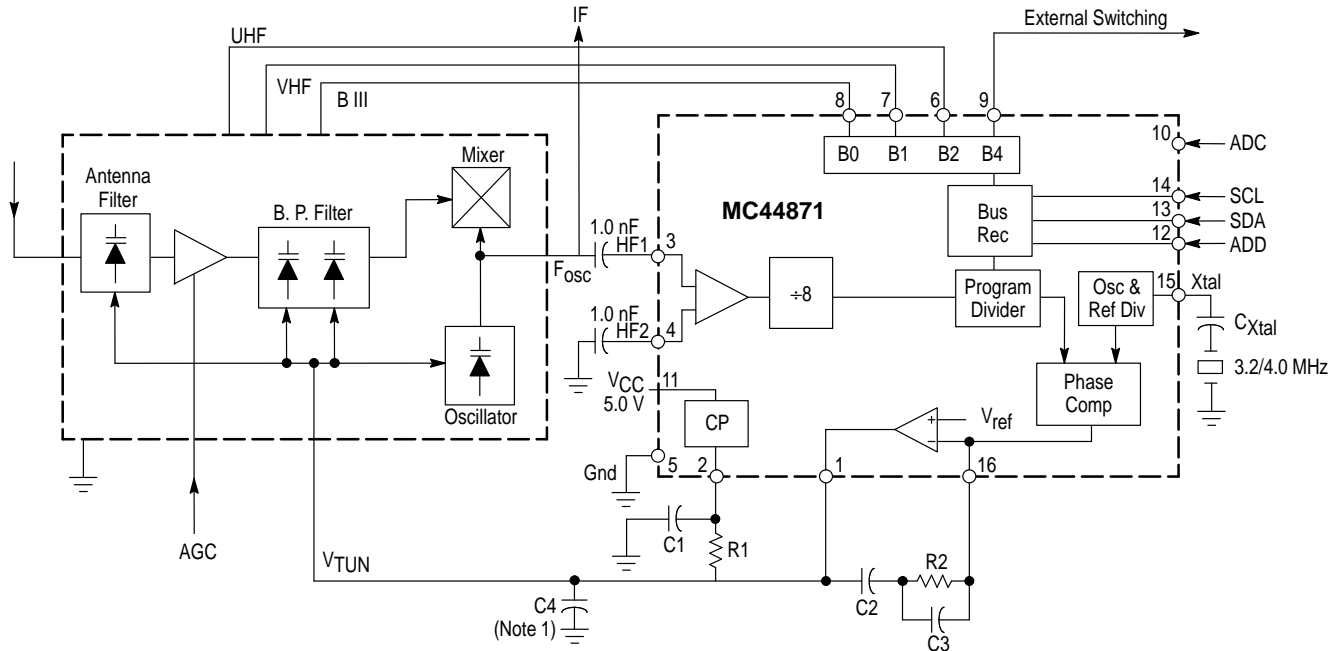
The typical power dissipation of the circuit is about 200 mW ($V_{TUN} = 15$ V with external pull-up of 560 k Ω , one buffer "On" at 30 mA). It is calculated with the following formula:

$$PD = (V_{CC} \times I_{CC}) + \frac{V_{Pin2} - V_{TUN}}{560 \text{ k}\Omega} \times V_{TUN} + (V_{sat} \times I_{Out})_{buffer}$$

$$\text{Example: } (5 \times 38) + \frac{32 - 15}{5.6 \times 10^5} \times 15 + (0.20 \times 30) = 197 \text{ mW}$$

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Figure 8. Typical Tuner Application



- NOTES:**
- 330 pF minimum is required for stability.
 - Approximate values of the external components for generation of the tuning voltage are:

| | |
|--|------------------------------|
| C1 = 1.0 nF | Charge Pump filter capacitor |
| R1 = 750 k Ω (560 k Ω minimum) | Pull-up resistor |
| C4 = 330 pF | VTUN filter capacitor |
| C2 = 47 nF | Loop Filter |
| C3 = 22 nF | Loop Filter |
| R2 = 39 k Ω | Loop Filter |

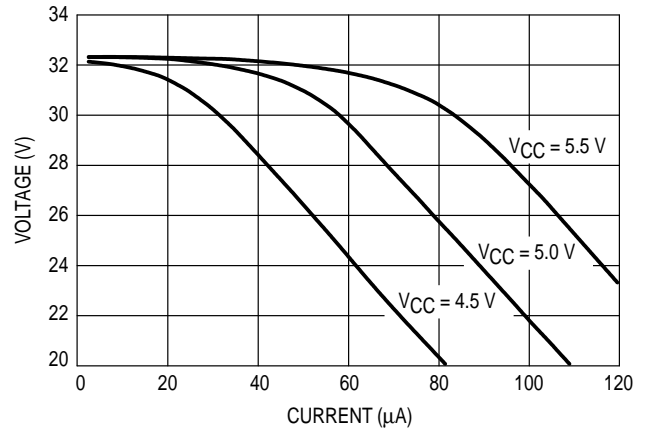
 These component values depend on the application.

DC-DC Converter Characteristics

The dc-to-dc converter block generates the 30 V supply voltage on the chip from VCC. Pin 2 only needs an external capacitor (1.0 nF) instead of an external 30 V supply. The charge pump switching frequency is taken from the oscillator.

Typical charge pump output current capability at 25°C is shown in Figure 9.

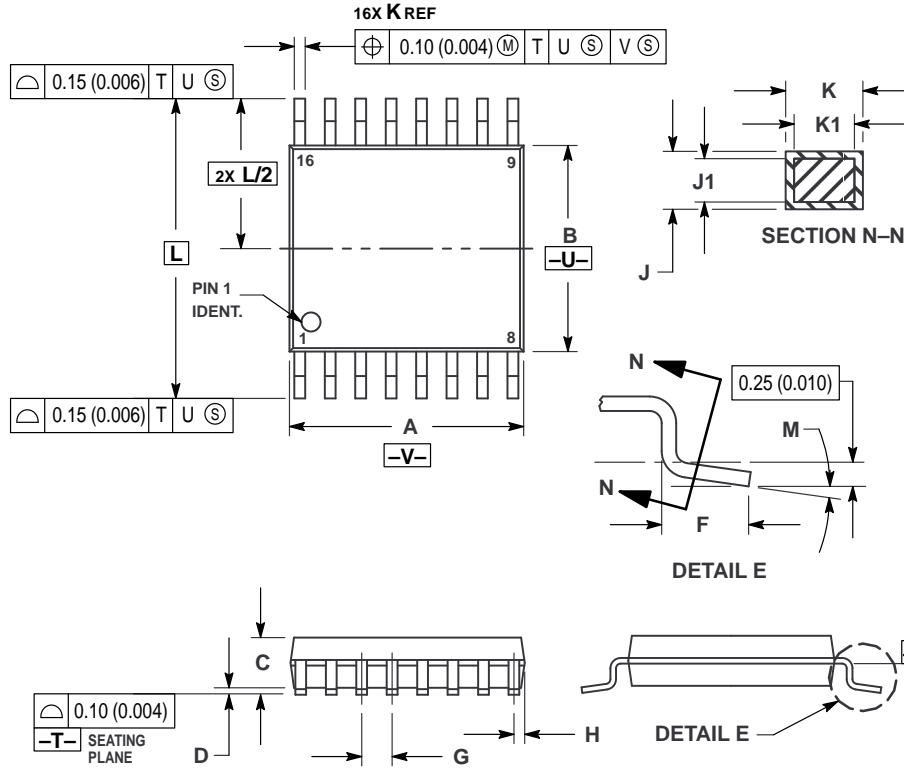
Figure 9. Typical Charge Pump Output Current



MC44871

OUTLINE DIMENSIONS


DTB SUFFIX
 PLASTIC PACKAGE
 CASE 948F-01
 (TSSOP-16)
 ISSUE O



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | — | 1.20 | — | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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