Preliminary

I. GENERAL DESCRIPTION

EM78P458 and EM78P459 are 8-bit microprocessors with low-power and high-speed CMOS technology. There is a 4096*13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM) within it.

Because of the OTP-ROM, the EM78P458 and EM78P459 offer users convenient ways to develop and verify their programs. Moreover, a user's developed code can be programmed easily by an EMC writer.

II. FEATURES

- Operating voltage range: 2.2V~6.0V
- Available in temperature range: 0°C~80°C
- Operating frequency range: DC ~ 16MHz
- Low power consumption:
  * less than 1.5 mA at 5V/4MHz
  * typical of 15 μA at 3V/32KHz
  * typical of 1 μA during the sleep mode
- 4096 x 13 bits on chip ROM
- 96 x 8 bits on chip registers (SRAM)
- 2 bi-directional I/O ports
- 8 level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges, and with overflow interrupt
- 8-bit multichannel Analog-to-Digital Converter with 13-bit resolution
- Dual Pulse Width Modulation (PWM) with 10-bit resolution
- One pair of comparators
- Power-down mode (SLEEP mode)
- Six available interruptions
  * TCC overflow interrupt
  * Input-port status changed interrupt (wake up from the sleep mode)
  * External interrupt
  * ADC completion interrupt
  * PWM period match completion
  * Comparator high interrupt
- Programmable free running watchdog timer
- 8 Programmable pull-down I/O pins
- 8 programmable pull-high I/O pins
- 8 programmable open-drain I/O pins
- Two clocks per instruction cycle
- 99.9% single instruction cycle commands
- Package type :
  * 20-pin DIP 300 mil : EM78P458AP
  * 20-pin SOP 300 mil : EM78P458AM
  * 24-pin DIP 300 mil : EM78P459AK
  * 24-pin SOP 300 mil : EM78P459AM
- Power on voltage detector available (2.0V ± 0.15V)

Preliminary

III. PIN ASSIGNMENTS

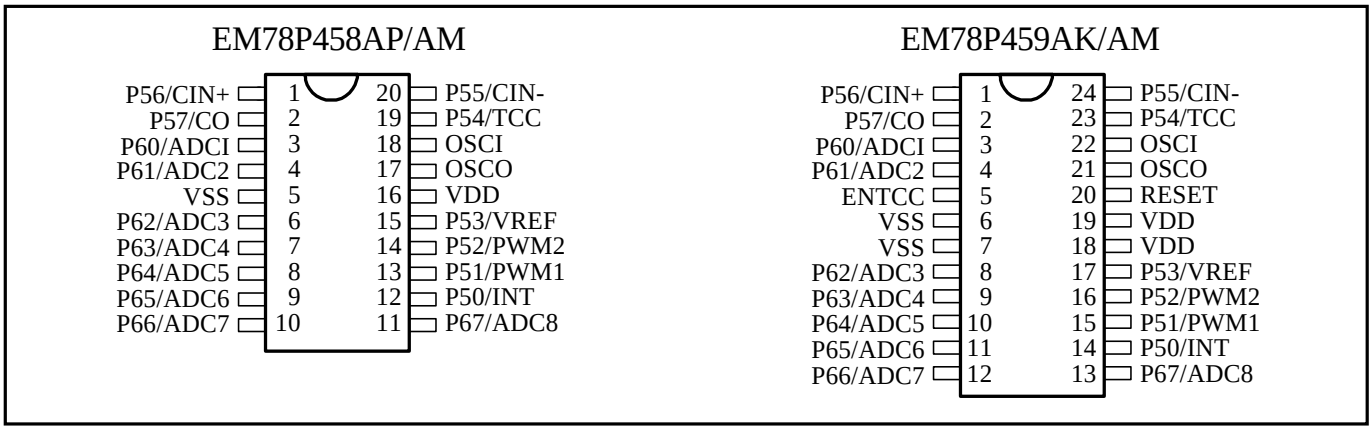

Fig. 1 Pin assignments

IV. FUNCTIONAL BLOCK DIAGRAM

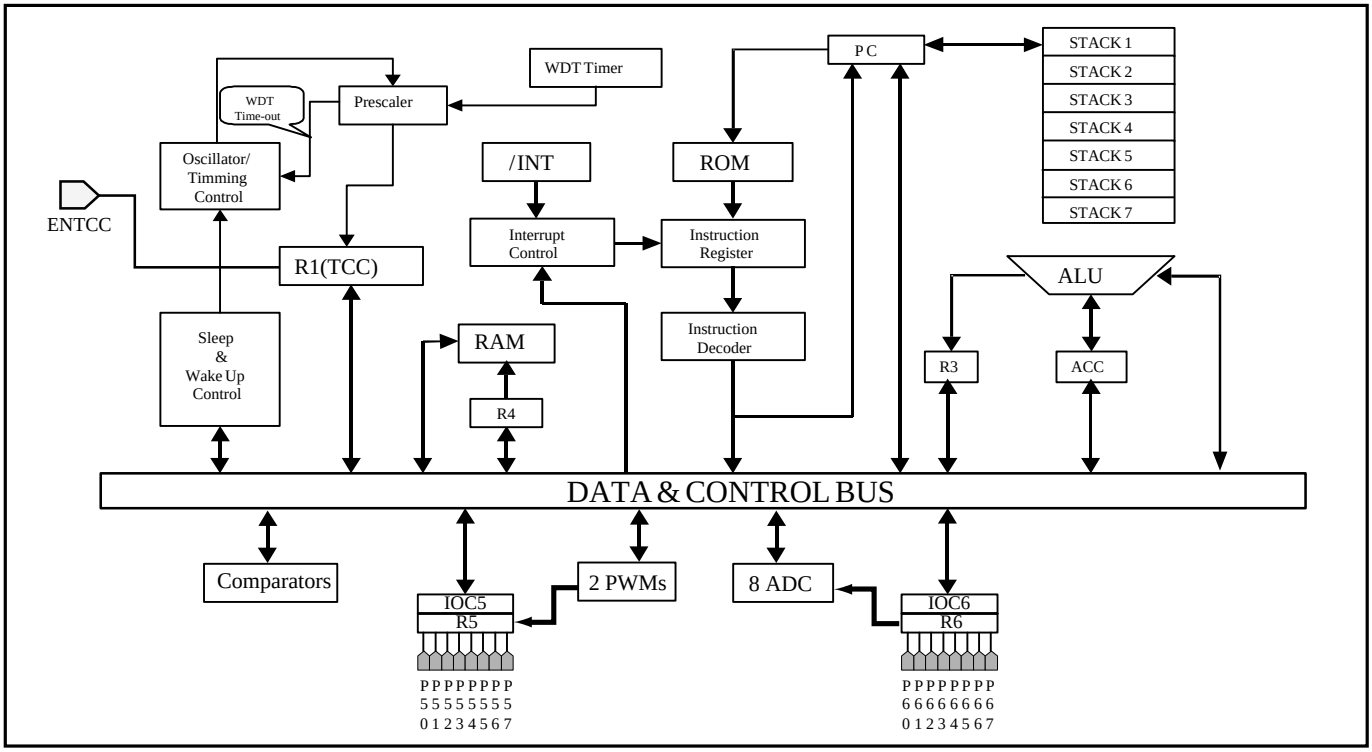

Fig. 2 Functional block diagram

V. PIN DESCRIPTION (EM78P458)

Table 1 Pin description-EM78P458

Symbol	Type	Function Description
VDD	-	Power supply.
OSCI	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.

Symbol	Type	Function Description
OSCO	O	* XTAL type: output terminal for crystal oscillator or external clock input pin. * RC type: clock output with a period of one instruction cycle time, the prescaler determined by the CONT register. * External clock signal input.
P50 ~ P57	I/O	* General-purpose I/O pin. * Default value while power -on reset.
P60 ~ P67	I/O	* General-purpose I/O pin. * Default value while power-on reset.
INT	I	* External interrupt pin triggered by falling edge.
ADC1~ADC8	I	* Analog to Digital Converter. * Defined by AD-CMPCON (IOCA0)<2:4>.
PWM1, PWM2	O	* Pulse width modulation outputs. * Defined by PWMCON (IOC51)<6, 7>
VREF	I	* External reference voltage for ADC * Defined by AD-CMPCON (IOCA0)<7>.
C-, C+ CO	I O	* "-" -> the input pin of Vin- of the comparator. * "+"-> the input pin of Vin+ of the comparator. * Pin CO is the output of the comparator. * Defined by AD-CMPCON (IOCA0) <5, 6>
TCC	I	Real time clock/counter with Schmitt trigger input pin; it must be tied to VDD or VSS if it is not in use.
VSS	-	Ground.

Table 2 Pin description-EM78P459

Symbol	Type	Function Description
VDD	-	* Power supply.
OSCI	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	O	* XTAL type: output terminal for crystal oscillator or external clock input pin. * RC type: clock output with a period of one instruction cycle times the prescaler determined by the CONT register. * External clock signal input.
P50 ~ P57	I/O	* General-purpose I/O pin. * Default value while power on reset.
P60 ~ P67	I/O	* General-purpose I/O pin. * Default value while power on reset.
/INT	I	* External interrupt pin triggered by falling edge.
ADC1~ADC8	I	* Analog to Digital Converter. * Defined by AD-CMPCON (IOCA0)<2:4>.
PWM1, PWM2	O	* Pulse width modulation outputs. * Defined by PWMCON (IOC51)<6, 7>
VREF	I	* External reference voltage for ADC * Defined by AD-CMPCON (IOCA0)<7>.
C-, C+	I	* '-' -> the Vin- input pins of the comparators.

Symbol	Type	Function Description
CO	O	* '+' -> the Vin+ input pins of the comparators. * Pin CO is the output of the comparator. * Defined by AD-CMPCON (IOCA0) <5, 6>
/RESET	I	* If remain at logic low, the device will be in reset. * Wake up from sleep mode while the status of the pin changed. * Voltage on /RESET/Vpp must not be over Vdd during the normal mode. * Pull-high is on if /RESET is asserted.
TCC	I	Real time clock/counter with Scmitt trigger input pin; it must be tied to VDD or VSS if it is not in use.
ENTCC	I	1: Enable TCC; 0: disable TCC.
VSS	-	Ground.

VI. FUNCTION DESCRIPTION

VI.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to be an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

2. R1 (Time Clock /Counter)

- Increased by an external signal edge through the TCC pin, or by the instruction cycle clock.
- The signals to increase the counter are decided by bit 4 and bit 5 of the CONT register.
- Writable and readable as any other registers.

3. R2 (Program Counter) & Stack

- R2 and hardware stacks are 12-bit wide. The structure is depicted in Fig. 4.
- Generating 4096x13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are set all "0"s upon a RESET condition.
- "JMP" instruction allows the direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can locate anywhere within a page.
- "RET" ("RETL K", "RETI") instruction loads the program counter with the contents of the top of stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction which would modify the contents of R2 (e.g. "ADD R2, A", "MOV R2, A", "BC R2, 6",.....) will cause the ninth bit and the tenth bit (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.

- In the case of EM78P458/EM78P459, the two most two significant bits (A11 and A10) will be loaded with the content of PS1 and PS0 in the status register (R3) upon the execution of a "JMP", "CALL", or any other instructions which would change the contents of R2.
- All instructions are single instruction cycle (fclk/2) except the instructions which would modify the contents of R2 need one more instruction cycle.

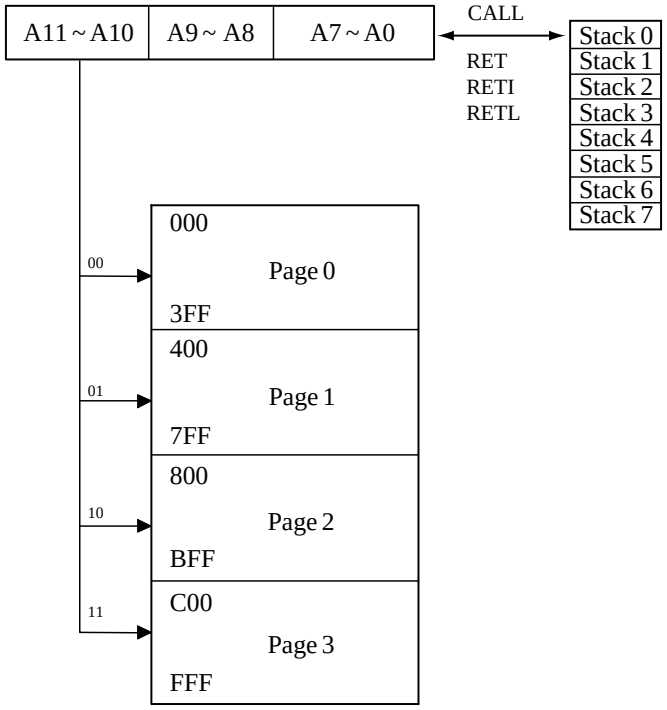

Fig. 3 Program counter organization

4. R3 (Status Register)

7	6	5	4	3	2	1	0
CMPOUT	PS1	PS0	T	P	Z	DC	C

- Bit 7 (CMPOUT) the result of the comparator.
- Bit 6 (PS1) ~ 5 (PS0) Page-selecting bits. PS0~PS1 are used to select a program memory page.
  When executing "JMP", "CALL", or other instructions which cause the program counter to be changed (e.g. MOV R2,A), PS0~PS1 are loaded to the 11th and 12th bits of the program counter which would select one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will be always to the page from the place where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

- Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands, or during power-up and reset to 0 by WDT time-out.
- Bit 3 (P) Power-down bit. Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
- Bit 1 (DC) Auxiliary carry flag.
- Bit 0 (C) Carry flag.

5. R4 (RAM Select Register)

- Bits 0~5 are used to select registers (address: 00~3F) in the indirect addressing mode.
- Bit 6 is used to select bank 0 or bank 1.
- Bit 7 is a general-purpose read/write bit.
- See the configuration of the data memory in Fig. 4.

6. R5 ~ R6 (Port 5 ~ Port 6)

- R5 and R6 are I/O registers.
- P50 can only be defined as input pin.

7. R7 ~ R8

- All of these are 8-bit general-purpose registers.

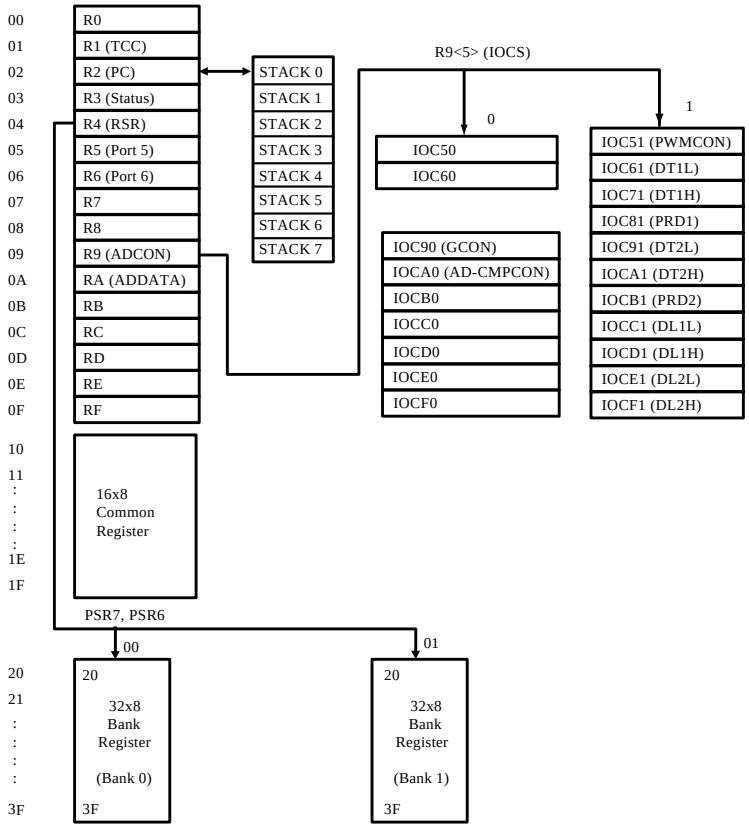

Fig. 4 Data memory configuration

8. R9 (ADCON: Analog to Digital Control)

7	6	5	4	3	2	1	0
-	-	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

- Bit 7~Bit 6 Unemployed, read as '0'.
- Bit 5(IOCS): Select the Segment of IO control register.
  1 = Segment 1(IOC51~IOCF1) selected.
  0 = Segment 0(IOC50~IOCF0) selected.
- Bit 4 (ADRUN): ADC starts to RUN.
  1 = an A/D conversion is started, this bit can be set by software.
  0 = reset on completion of the conversion, this bit can not be reset in software.
- Bit 3 (ADPD): ADC Power-down mode.
  1 = ADC is operating.
  0 = switch off the resistor reference to save the power even the CPU is operating.
- Bit2~Bit0 (ADIS2~ADIS0): Analog Input Select.
  000 = AN0;
  001 = AN1;
  010 = AN2;
  011 = AN3;
  100 = AN4;
  101 = AN5;
  110 = AN6;
  111 = AN7;
  They only can be changed when the ADIF bit and the ADRUN bit are both LOW.

9. RA (ADDATA: the converted value of ADC)

- When the A/D conversion is complete, the result is loaded to the ADDATA. The START//END bit is clear, and the ADIF is set.

10. RB

- An 8-bit general-purpose register.

11. RC

- A two-bit, bit 0 and bit 1, register.

12. RD

- An 8-bit general-purpose register.

13. RE

- A two-bit, bit 0 and bit 1, register.

14. RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	CMPIF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

- "1" means interrupt request, and "0" means non-interrupt occurrence.
- Bit 0 (TCIF) TCC overflowing interrupt flag. Set when TCC overflows, reset by software.
- Bit 1 (ICIF) Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.
- Bit 2 (EXIF) External interrupt flag. Set by falling edge on /INT pin, reset by software.
- Bit 3 (ADIF) Interrupt flag for analog to digital conversion. Set while AD conversion finished, reset by software.
- Bit 4 (PWM1IF) PWM1 (Pulse Width Modulation) interrupt flag. Set while a selected period reached, reset by software.
- Bit 5 (PWM2IF) PWM2 (Pulse Width Modulation) interrupt flag. Set while a selected period reached, reset by software.
- Bit 6 (CMPIF) High-Compared interrupt flag. Set as there is a change in the output of the comparator, reset by software.
- Bit 7 Unemployed, read as '0';
  * RF can be cleared by instruction but can not be set.
  * IOCF0 is the interrupt mask register.
  * Note that the result of reading RF is the "logic AND" of RF and IOCF0.

15. R10 ~ R3F

- All of these are 8-bit general-purpose registers.

VI.2 Special Purpose Registers

1. A (Accumulator)

- Internal data transfer, or instruction operand holding.
- It can not be addressed.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
INTE	INT	TS	TE	PAB	PSR2	PSR1	PSR0

- Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- Bit 3 (PAB) Prescaler assignment bit.

  0: TCC

  1: WDT
- Bit 4 (TE) TCC signal edge
  0: increment if the transition from low to high takes place on the TCC pin;
  1: increment if the transition from high to low takes place on the TCC pin.
- Bit 5 (TS) TCC signal source
  0: internal instruction cycle clock; if P54 is used as an I/O pin, TS must be 0.
  1: transition on the TCC pin
- Bit 6 (INT) Interrupt enable flag
  0: masked by DISI or hardware interrupt
  1: enabled by the ENI/RETI instruction
- Bit 7 (INTE) INT signal edge
  0: interrupt occurs at the rising edge on the INT pin
  1: interrupt occurs at the falling edge on the INT pin
- CONT register is both readable and writable.

3. IOC50 ~ IOC60 (I/O Port Control Register)

- "1" puts the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.
- IOC50 and IOC60 registers are both readable and writable.
- Bit0 of IOC50 can only be set to “1”, i.e. input pin.

4. IOCB0 (Pull-down Control Register)

7	6	5	4	3	2	1	0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

- Bit 0 (/PD0) Control bit used to enable the pull-down of the P60 pin.
  0: Enable internal pull-down;
  1: Disable internal pull-down.
- Bit 1 (/PD1) Control bit used to enable the pull-down of the P61 pin.
- Bit 2 (/PD2) Control bit used to enable the pull-down of the P62 pin.
- Bit 3 (/PD3) Control bit used to enable the pull-down of the P63 pin.
- Bit 4 (/PD4) Control bit used to enable the pull-down of the P64 pin.
- Bit 5 (/PD5) Control bit used to enable the pull-down of the P65 pin.
- Bit 6 (/PD6) Control bit used to enable the pull-down of the P66 pin.
- Bit 7 (/PD7) Control bit used to enable the pull-down of the P67 pin.
- IOCB0 register is both readable and writable.

5. IOCC0 (Open-drain Control Register)

7	6	5	4	3	2	1	0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

- Bit 0 (OD0) Control bit used to enable the open-drain of the P64 pin.
  0: Enable open-drain output.
  1: Disable open-drain output.

- Bit 1 (OD1) Control bit used to enable the open-drain of the P65 pin.
- Bit 2 (OD2) Control bit used to enable the open-drain of the P66 pin.
- Bit 3 (OD3) Control bit used to enable the open-drain of the P67 pin.
- Bit 4 (OD4) Control bit used to enable the open-drain of the P51 pin.
- Bit 5 (OD5) Control bit used to enable the open-drain of the P52 pin.
- Bit 6 (OD6) Control bit used to enable the open-drain of the P54 pin.
- Bit 7 (OD7) Control bit used to enable the open-drain of the P57 pin.
- IOCC0 register is both readable and writable.

6. IOCD0 (Pull-high Control Register)

7	6	5	4	3	2	1	0
/PH7	/PH6	/PH5	-	/PH3	/PH2	/PH1	/PH0

- Bit 0 (/PH0) Control bit used to enable the pull-high of the P60 pin.
  0: Enable internal pull-high.
  1: Disable internal pull-high.
- Bit 1 (/PH1) Control bit used to enable the pull-high of the P61 pin.
- Bit 2 (/PH2) Control bit used to enable the pull-high of the P62 pin.
- Bit 3 (/PH3) Control bit used to enable the pull-high of the P63 pin.
- Bit 4 Not used.
- Bit 5 (/PH5) Control bit used to enable the pull-high of the P53 pin.
- Bit 6 (/PH6) Control bit used to enable the pull-high of the P55 pin.
- Bit 7 (/PH7) Control bit used to enable the pull-high of the P56 pin.
- IOCD0 register is both readable and writable.

7. IOCE0 (WDT Control Register)

7	6	5	4	3	2	1	0
WDTE	EIS	-	-	-	-	-	-

- Bit 7 (WDTE) Control bit used to enable Watchdog Timer.
  0: Disable WDT.
  1: Enable WDT.
- WDTE is both readable and writable.
- Bit 6 (EIS) Control bit used to define the function of the P50 (/INT) pin.
  0: P50, input pin only.
  1: /INT, external interrupt pin. In this case, the I/O control bit of P50 (bit 0 of IOC50) must be set to "1".
- When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 5 (R5). Refer to Fig. 7.
- EIS is both readable and writable.
- Bits 0~5 Not used.

8. IOCF0 (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	CMPIE	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

- Bit 0 (TCIE) TCIF interrupt enable bit.
  0: disable TCIF interrupt
  1: enable TCIF interrupt
- Bit 1 (ICIE) ICIF interrupt enable bit.
  0: disable ICIF interrupt
  1: enable ICIF interrupt
- Bit 2 (EXIE) EXIF interrupt enable bit.
  0: disable EXIF interrupt
  1: enable EXIF interrupt
- Bit 3 (ADIE) ADIF interrupt enable bit.
  0: disable ADIF interrupt
  1: enable ADIF interrupt
- Bit 4 (PWM1IE) PWM1IF interrupt enable bit.
  0: disable PWM1 interrupt
  1: enable PWM1 interrupt
- Bit 5 (PWM2IE) PWM2IF interrupt enable bit.
  0: disable PWM2 interrupt
  1: enable PWM2 interrupt
- Bit 6 (CMPIE) CMPIF interrupt enable bit.
  0: disable CMPIF interrupt
  1: enable CMPIF interrupt
- Bit 7: Unimplemented, read as '0'.
  - Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "1".
  - Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 8.
  - IOCF0 register is both readable and writable.

9. IOC90 (GCON: I/O configuration & control of ADC)

7	6	5	4	3	2	1	0
OP2E	OP1E	G42	G41	G40	G12	G11	G10

- Bit 7 (OP2E) Enable the gain amplifier whose input is connected to P64 and output is connected to the 8-1 analog switch.
  0 = OP2 is off (default value), and bypasses the input signal to the ADC;
  1 = OP2 is on.
- Bit 6 (OP1E) Enable the gain amplifier whose input is connected to P60 and output is connected to the 8-1 analog switch.
  0 = OP1 is off (default value), and bypasses the input signal to the ADC;

1 = OP1 is on.

- Bit 5~Bit 3 (G42 and G40): Select the gain of OP2.
  000 = IS x 1 (default value);
  001 = IS x 2;
  010 = IS x 4;
  011 = IS x 8;
  100 = IS x 16;
  101 = IS x 32;
  Legend: IS = the input signal
- Bit 2~Bit 0 (G12 and G10): Select the gain of OP1.
  000 = IS x 1 (default value);
  001 = IS x 2;
  010 = IS x 4;
  011 = IS x 8;
  100 = IS x 16;
  101 = IS x 32;
  Legend: IS = the input signal

10. IOCA0 (AD-CMPCON):

7	6	5	4	3	2	1	0
VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0

- Bit 7: The input source of the Vref of the ADC.
  0 = The Vref of the ADC is connected to Vdd (default value), the P53/VREF pin carries out the function of P53.
  1 = The Vref of the ADC is connected to P53/VREF.
- Bit 6 (CE): Comparator enable bit
  0 = Comparator is off (default value).
  1 = Comparator is on.
- Bit 5 (COE): Set P57 as the output of the comparator
  0 = the comparator acts as an OP if CE=0.
  1 = act as a comparator if CE=1
- Bit4~Bit2 (IMS2~IMS0):
  Input Mode Select. ADC configuration definition bit. The following Table describes how to define the characteristic of each pin of R6.

Table 3 The description of AD configuration control bits

IMS2~IMS0	P60	P61	P62	P63	P64	P65	P66	P67
000	A	D	D	D	D	D	D	D
001	A	A	D	D	D	D	D	D
010	A	A	A	D	D	D	D	D
011	A	A	A	A	D	D	D	D
100	A	A	A	A	A	D	D	D
101	A	A	A	A	A	A	D	D
110	A	A	A	A	A	A	A	D
111	A	A	A	A	A	A	A	A

- Bit 1~ Bit 0 (CKR1~ CKR0): The prescaler of oscillator clock rate of ADC
  00 = 1: 4 (default value);
  01 = 1: 16;
  10 = 1: 64;
  11 = 1: WDT ring oscillator frequency.

11. IOC51 (PWMCON):

7	6	5	4	3	2	1	0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

- Bit 7 (PWM2E): PWM2 enable bit
  0 = PWM2 is off (default value), and its related pin carries out the function of P52.
  1 = PWM2 is on, and its related pin will be set to output automatically.
- Bit 6 (PWM1E): PWM1 enable bit
  0 = PWM1 is off (default value), and its related pin carries out the function of P51.
  1 = PWM1 is on, and its related pin will be set to output automatically.
- Bit 5 (T2EN): TMR2 enable bit
  0 = TMR2 is off (default value).
  1 = TMR2 is on.
- Bit 4 (T1EN): TMR1 enable bit
  0 = TMR1 is off (default value).
  1 = TMR1 is on.
- Bit 3~Bit 2 (T2P1~T2P0): TMR2 clock prescale option bits.

T2P1	T2P0	Prescale
0	0	1:2(Default)
0	1	1:8
1	0	1:32
1	1	1:64

- Bit 1 ~ Bit 0 (T1P1~T1P0): TMR1 clock prescale option bits.

T1P1	T1P0	Prescale
0	0	1:2(Default)
0	1	1:8
1	0	1:32
1	1	1:64

12. IOC61 (DT1L: the Least Significant Byte, Bit 7 ~ Bit 0, Duty Cycle of PWM1)

- A specified value keeps the output of PWM1 stay at high until the value matches with TMR1.

13. IOC71 (DT1H: the Most Significant Byte, Bit 1 ~ Bit 0, Duty Cycle of PWM1)

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7	6	5	4	3	2	1	0
CALI1	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	-	PWM1[9]	PWM1[8]

- Bit 7 (CALI1): Calibration enable bit
  0 = Calibration disable.
  1 = Calibration enable.
- Bit 6 (SIGN1): Polarity bit of offset voltage
  0 = Negative voltage.
  1 = Positive voltage.
- Bit 5~Bit 3 (VOF1[2]~VOF1[0]): Offset voltage bits.
- Bit 1~Bit 0 (PWM1[9]~PWM1[8]): The Most Significant Byte of Duty Cycle of PWM1

  A specified value keeps the output of PWM1 stay at high until the value matches with TMR1.

14. IOC81 (PRD1: Period of PWM1):

The content of IOC81 is a period of PWM1. The frequency of PWM1 is the reverse of the period.

15. IOC91 (DT2L: the Least Significant Byte, Bit 7 ~ Bit 0, Duty Cycle of PWM2)

A specified value keeps the output of PWM2 stay at high until the value matches with TMR2.

16. IOCA1 (DT2H: the Most Significant Byte, Bit 1 ~ Bit 0, Duty Cycle of PWM2)

7	6	5	4	3	2	1	0
CALI2	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	-	PWM2[9]	PWM2[8]

- Bit 7 (CALI2): Calibration enable bit
  0 = Calibration disable.
  1 = Calibration enable.
- Bit 6 (SIGN2): Polarity bit of offset voltage
  0 = Negative voltage.
  1 = Positive voltage.
- Bit 5~Bit 3 (VOF2[2]~VOF2[0]): Offset voltage bits
- Bit 1~Bit 0 (PWM2[9]~PWM2[8]): The Most Significant Byte of Duty Cycle of PWM2

- A specified value keeps the output of PWM2 stay at high until the value matches with TMR2.

17. IOCB1 (PRD2: Period of PWM2)

- The content of IOCB1 is a period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

18. IOCC1 (DL1L: the Least Significant Byte, Bit 7 ~ Bit 0, of Duty Cycle Latch of PWM1)

- The content of IOCC1 is read-only.

19. IOCD1 (DL1H: the Most Significant Byte, Bit 1 ~ Bit 0, of Duty Cycle Latch of PWM1)

- The content of IOCD1 is read-only.

20. IOCE1 (DL2L: the Least Significant Byte, Bit 7 ~ Bit 0, of Duty Cycle Latch of PWM2)

- The content of IOCE1 is read-only.

21. IOCF1 (DL2H: the Most Significant Byte, Bit 1 ~ Bit 0, of Duty Cycle Latch of PWM2)

- The content of IOCF1 is read-only.

VI.3 TCC/WDT Presacler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available only for either the TCC or the WDT at the same time and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler will be cleared by the instructions which write to TCC each time, when assigned to TCC mode. The WDT and prescaler, when assigned to the WDT mode, will be cleared by the "WDTC" and "SLEP" instructions. Fig. 5 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 in every instruction cycle (without prescaler). Refer to Fig. 5, CLK=Fosc/2 or CLK=Fosc/4 is depended on the CODE Option bit CLKS. CLK=Fosc/2 if CLKS bit is "0", and CLK=Fosc/4 if CLKS bit is "1".

- If TCC signal source is from external clock input, TCC will increase by 1 on every falling edge or rising edge of TCC pin.

- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of IOCE0 register. With no presacler, the WDT time-out period is approximately 18 ms.

VI.4 I/O Ports

Port 5, Port 6 and the I/O registers are bi-directional tri-state I/O ports. The function of Pull-high, Pull-down, and Open-drain can be set internally by IOCB0, IOCC0 and IOCD0 respectively. There is an input status changed interrupt (or wake-up) function on Port 6. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC60). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in Fig. 6 and Fig. 7(a),(b) respectively.

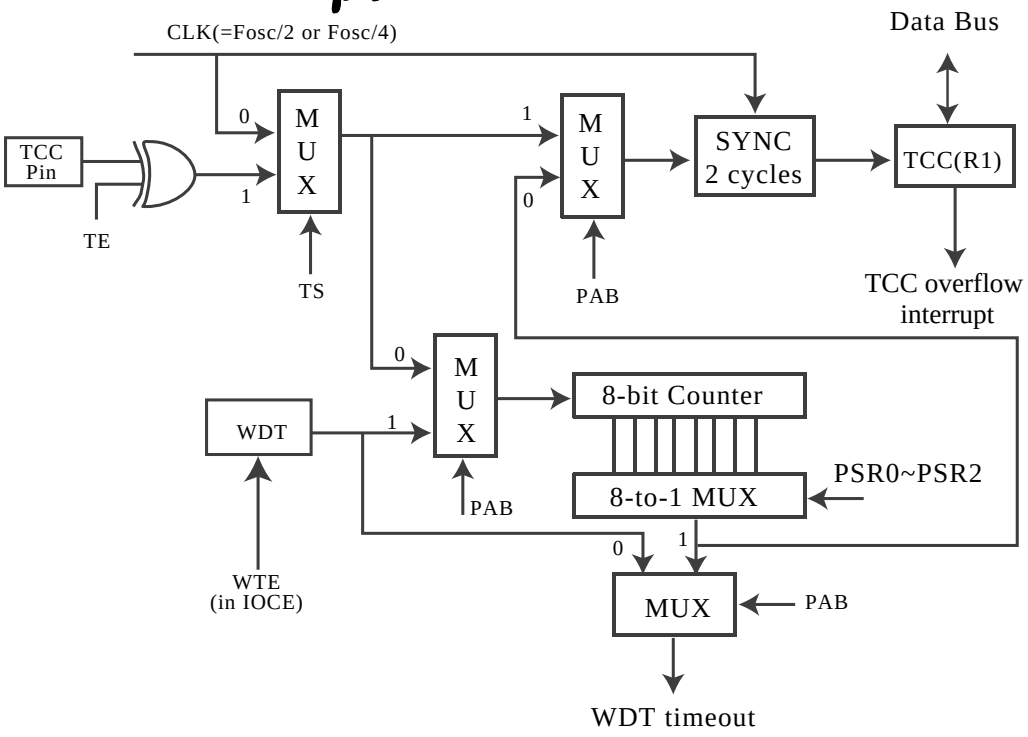
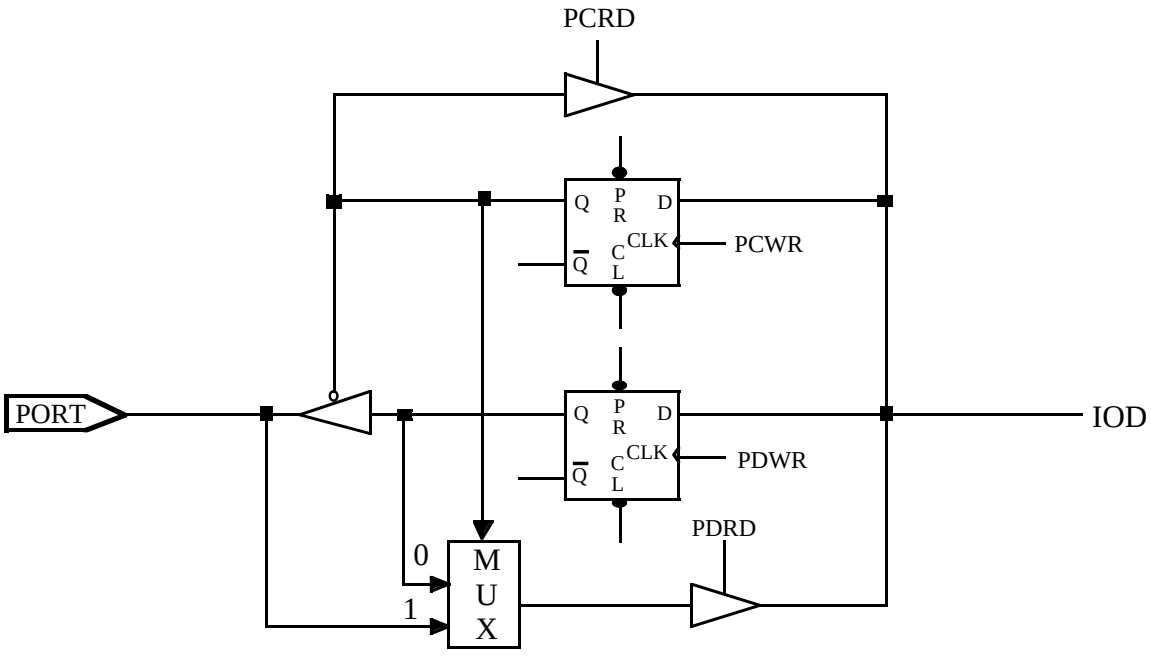


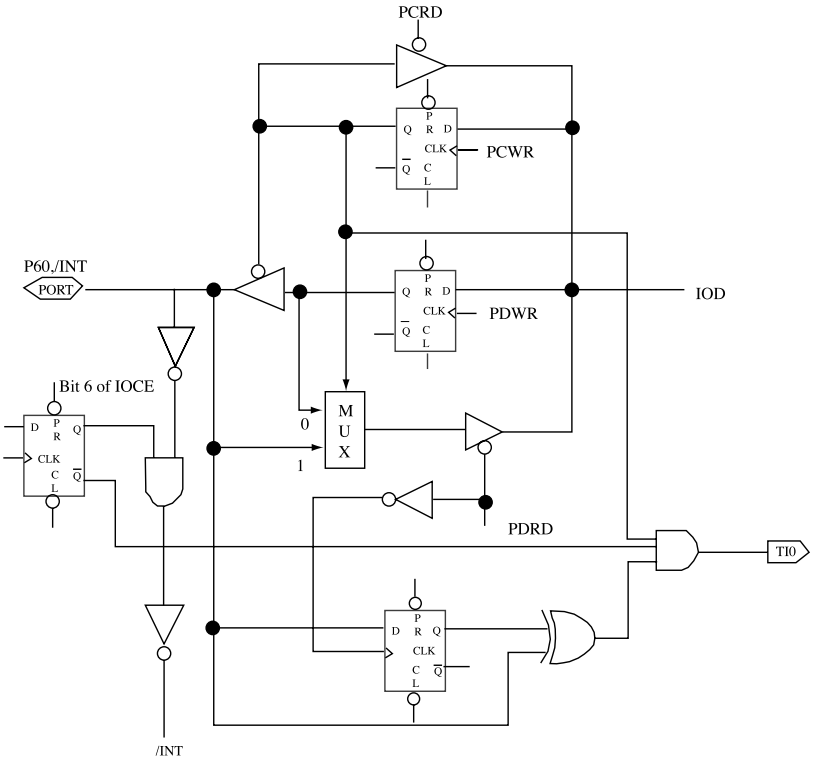
Fig. 5 Block diagram of TCC and WDT



*Pull-down is not shown in the figure.

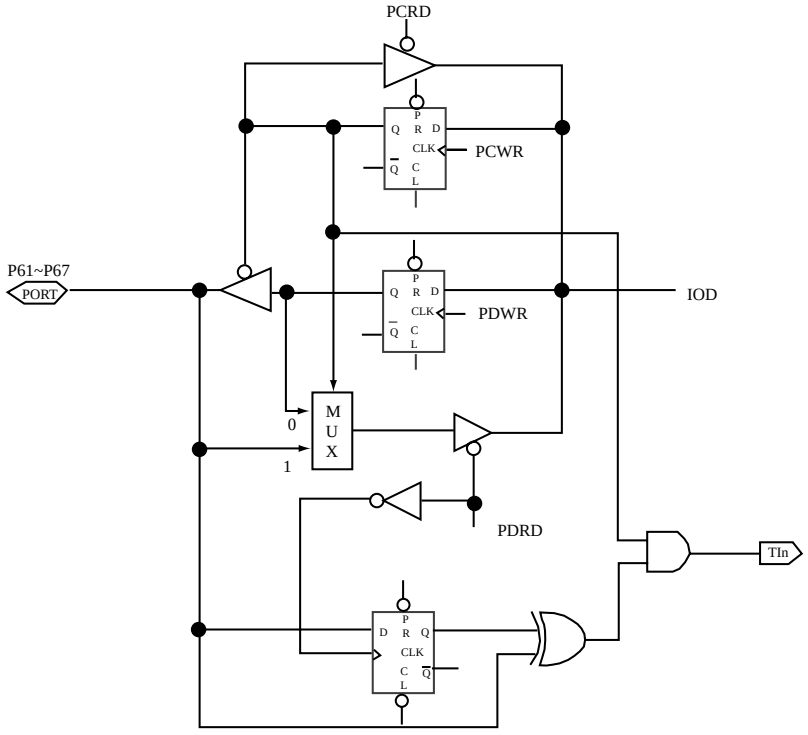
Fig. 6 The circuit of I/O port and I/O control register for Port 5

Preliminary



*Pull-high (down) and open-drain are not shown in the figure.

Fig. 7(a) The circuit of I/O port and I/O control register for P50(/INT)



*Pull-high (down) and open-drain are not shown in the figure.

Fig. 7(b) The circuit of I/O port and I/O control register for P60~P67

Preliminary

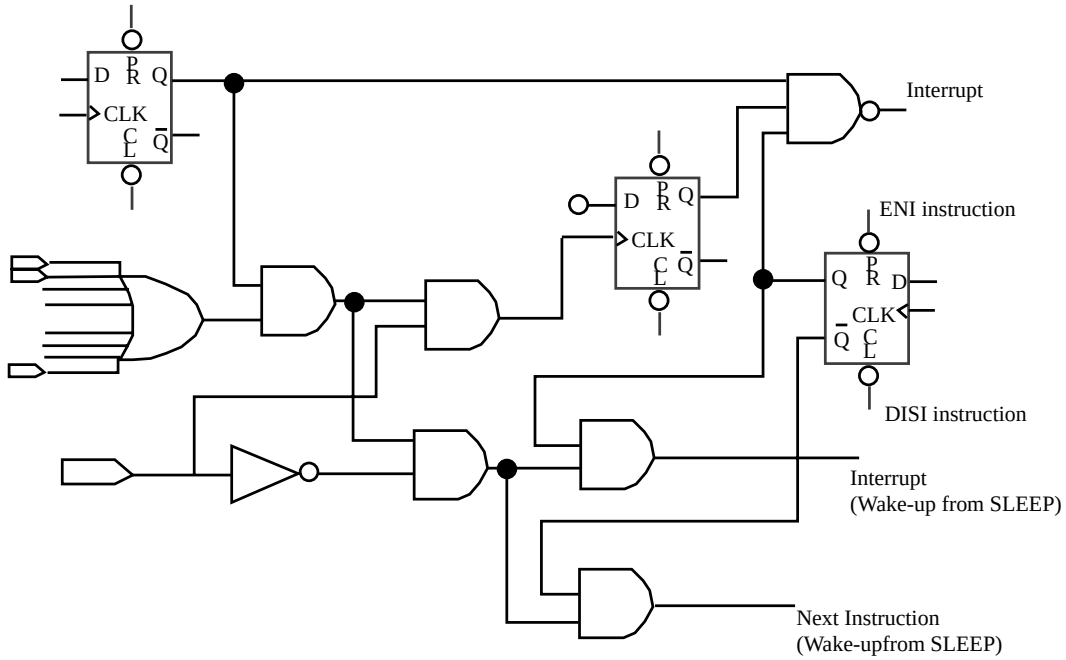


Fig. 8(c) Block diagram of Port 6 with input changed interrupt/wake-up

Table 4 Usage of port 6 input changed wake-up/interrupt function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 input status changed (a) Before SLEEP 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF0.1) 5. Execute "SLEP" instruction (b) After wake-up 1. If "ENI" → Interrupt vector (008H) 2. If "DISI" → Next instruction	(II) Port 6 input status changed interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF0.1) 4. If Port 6 changed (interrupt) → Interrupt vector (008H)

VI.5 RESET and Wake-up

1. The Function of RESET and Wake-up

The RESET can be caused by

(1) Power-on reset
(2) /RESET pin input "low", or
(3) WDT time-out (if enabled).

Note that only power-on reset, or only voltage detector in Case(1) is enabled in the system by CODE option bit. Refer to Fig. 9. The device will be kept in a RESET condition for a period of approx. 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- Upon power-on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except the bit 6 (INT flag).
- The bits of the IOCB0 register are set to all "1".
- The IOCC0 register is cleared.
- The bits of the IOCD0 register are set to all "1".
- Bit 7 of the IOCE0 register is set to "1", and Bits 6 is cleared.
- Bits 0~6 of RF register and bits 0~6 of IOCF0 register are cleared.

Executing the "SLEP" instruction can perform the sleep mode (power-down mode). While entering sleep mode, WDT (if enabled) is cleared but keeps running. The controller can be awakened by

(1) External reset input on /RESET pin.
(2) WDT time-out (if enabled).
(3) Port 6 input status changed (if enabled).
(4) Comparator high.
(5) ADC complete.

The first two cases will cause the EM78P458/EM78P459 to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3 is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 0x8 after wake-up. If DISI is executed before SLEP, the instruction will restart from the place where is right next to SLEP after wake-up.

Only one of the case2, case3, case4 and case5 can be enabled before entering the sleep mode. That is,

[a] if Port 6 input status changed interrupt is enabled before SLEP , WDT must be disabled by software; however, the WDT bit in the option register is still enabled. Hence, the EM78P458/EM78P459 can be awakened only by case 1 or 3.

[b] if WDT is enabled before SLEP, Port 6 input status changed interrupt must be disabled. Hence, the EM78P458/EM78P459 can be awakened only by case 1 or 2. Refer to the section on interrupt.

[c] if comparator high interrupt is enabled before SLEP , WDT must be disabled by software; however, the WDT bit in the option register is still enabled. Hence, the EM78P458/EM78P459 can be awakened only by case 1 or 4.

[d] if ADC complete interrupt is enabled before SLEP , WDT must be disabled by software; however, the WDT bit in the option register is still enabled. Hence, the EM78P458/EM78P459 can be awakened only by case 1 or 5.

If Port 6 input status changed interrupt is used to wake up the EM78P458/EM78P459 (the case [a]), the following instructions must be executed before SLEP:

```
MOV A, 0bxx000110          ; Select internal TCC clock
CONTW
CLR R1                     ; Clear TCC and prescaler
MOV A, 0bxxxx1110          ; Select WDT prescaler
```

```
CONTW
WDTC                    ; Clear WDT and prescaler
MOV A, 0b0xxxxxxx       ; Disable WDT
IOW RE
MOV R6, R6              ; Read Port 6
MOV A, 0b00000x1x       ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)           ; Enable (or disable) global interrupt
SLEP                    ; Sleep
NOP
```

In a similar way, if the comparator high interrupt is used to wake up the EM78P458/EM78P459 (the case [a]), the following instructions must be executed before SLEP:

```
MOV A, 0bxx000110       ; Select internal TCC clock
CONTW
CLR R1                  ; Clear TCC and prescaler
MOV A, 0bxxxx1110       ; Select WDT prescaler
CONTW
WDTC                    ; Clear WDT and prescaler
MOV A, 0b0xxxxxxx       ; Disable WDT
IOW RE
MOV A, 0b01xxxxxx       ; Enable comparator high interrupt
IOW RF
ENI (or DISI)           ; Enable (or disable) global interrupt
SLEP                    ; Sleep
NOP
```

One problem must be aware that after waking up from the sleep mode, the WDT function will enable automatically. The WDT operation (being enabled or disabled) should be handled appropriately by software after waking up from the sleep mode.

2. The status of T and P of STATUS register

A RESET condition can be caused by the following events:

(1) A power-on condition,
(2) A high-low-high pulse on /RESET pin, and
(3) Watchdog Timer time-out.

The values of T and P, listed in Table 5 can be used to check how the processor wakes up. Table 6 shows the events which may affect the status of T and P.

Table 5 The values of T and P after RESET

Reset Type	T	P
Power-on	1	1
/RESET during operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-up on pin changed during SLEEP mode	1	0

*P: Previous status before reset

Table 6 The status of T and P being affected by events

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during SLEEP mode	1	0

*P: Previous value before reset

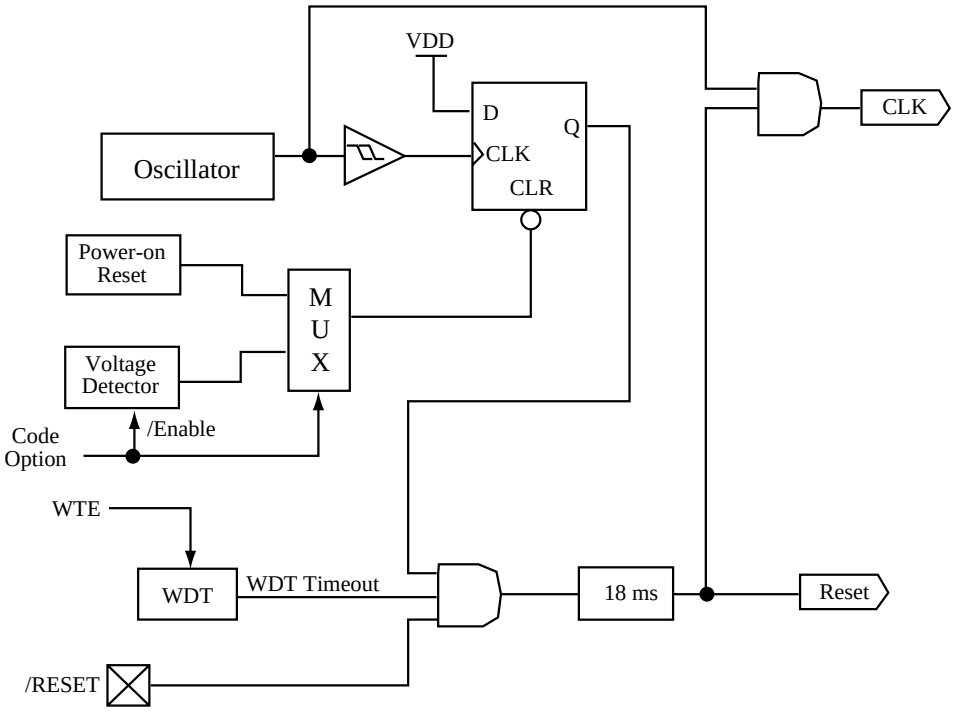


Fig. 9 Block diagram of Reset of controller

VI.6 Interrupt

The EM78P458/EM78P459 has six interrupts listed below:

Preliminary

(1) TCC overflow interrupt
(2) Port 6 input status changed interrupt
(3) External interrupt [(P50, /INT) pin].
(4) Analog to Digital converting complete (see VI.7).
(5) When TMR1/TMR2 matches with PRD1/PRD2 respectively in PWM (see VI.8).
(6) When any output of comparators is high (see VI.9).

Before Port 6 input status changed interrupt being enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each pin of Port 6 can have this feature if its status changes. Any pin configured as output or P50 pin configured as /INT is excluded from this function. Port 6 input status changed interrupt can wake up the EM78P458/EM78P459 from the sleep mode if it is enabled prior to going into the sleep mode by executing SLEP. When the controller is woken up, it will continue to execute the successive address if the global interrupt is disabled or branch to the interrupt vector 008H if the global interrupt is enabled.

RF, the interrupt status register, records the interrupt requests in the relative flags/bits. IOCF0 is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF0. Refer to Fig. 10. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (when enabled), the next instruction will be fetched from address 001H.

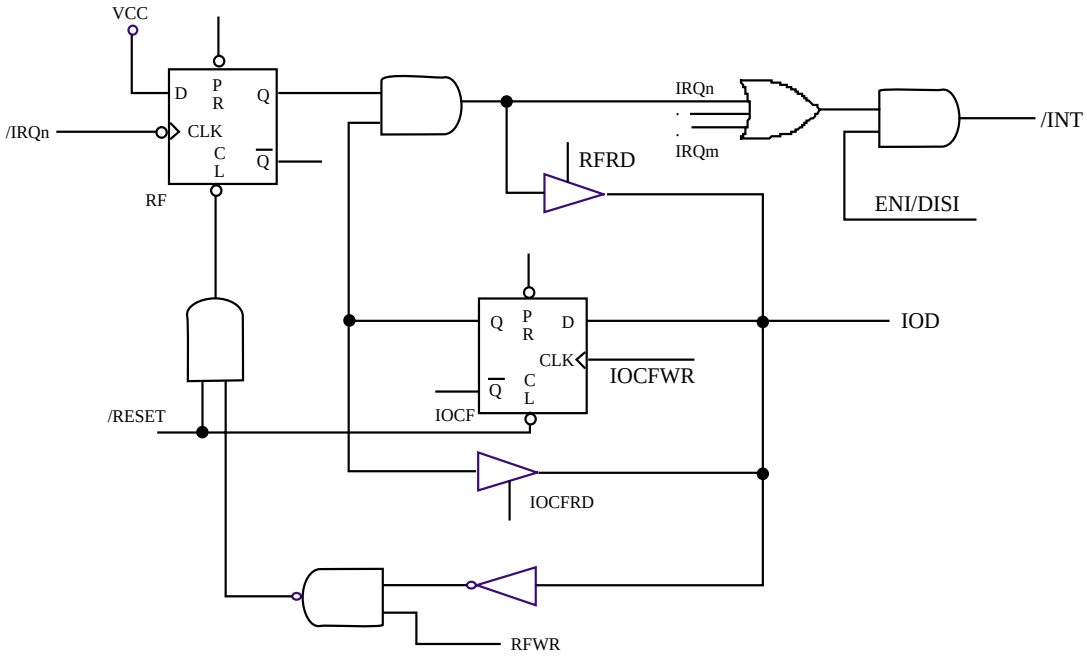


Fig. 10 Interrupt input circuit

VI.7 Analog-To-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer, three control registers (ADCON/R9, AD-CMP-CON/IOCA0, GCON/IOC90 shown), one data register (ADDATA/RA) and ADC with 8-bit resolution.
The functional block diagram of the ADC is shown in Fig. 11. The analog reference voltage (Vref) and analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal to a digital value.
The result is fed to the ADDATA. Input channels are selected by the analog input multiplexer via the ADCON register bits ADIS0, ADIS1 and ADIS2.

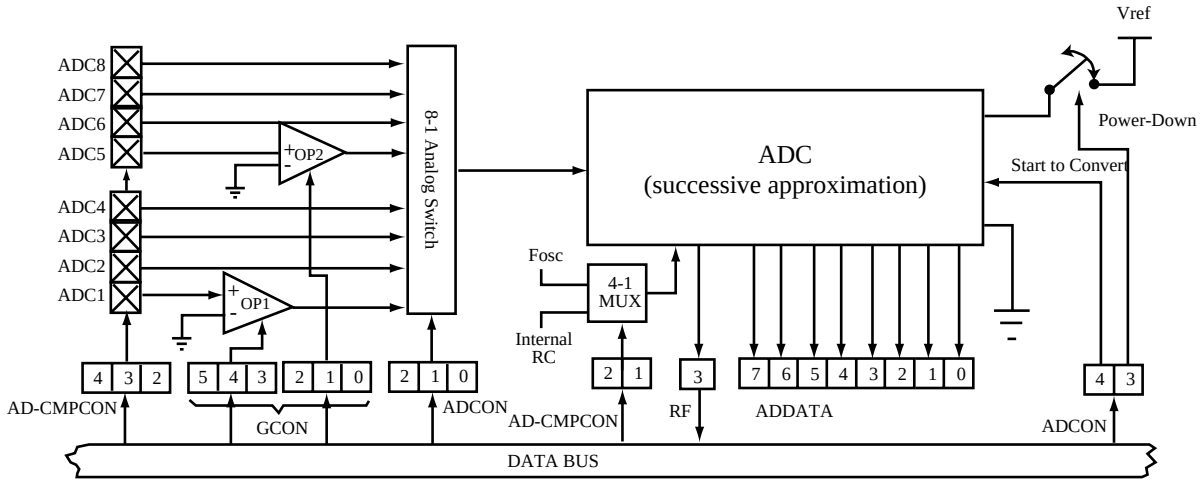


Fig. 11 The functional block diagram of analog-to-digital conversion

1. ADC Control register (ADCON/R9, AD-CMP-CON/IOCA0, GCON/IOC90)

1.1 ADCON/R9

The ADCON register controls the operation of the A/D conversion and decides which pin is active currently.
Table 7 shows the description of ADCON bits.

Table 7 The description of ADCON bits

BIT	7	6	5	4	3	2	1	0
SYMBOL	-	-	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
*Init_Value	0	0	0	0	0	0	0	0

* Init_Value: initial value at power on reset

IOCS (bit5) : I/O Register Selector
1 = Bank 1 of I/O registers, IOCx1
0 = Bank 0 of I/O registers, IOCx0

ADRUN (bit 4): ADC starts to RUN.
1 = an A/D conversion is started, this bit can be set by software.
0 = reset on completion of the conversion; this bit can not be reset in software.

ADPD (bit 3): ADC Power-down Mode.
1 = ADC is operating.
0 = switch off the resistor reference to save the power even the CPU is operating.

ADIS2~ADIS0 (bit 2~0): Analog Input Select.

000 = AN0;
001 = AN1;
010 = AN2;
011 = AN3;
100 = AN4;
101 = AN5;
110 = AN6;
111 = AN7;

They only can be changed when the ADIF bit and the ADRUN bit are both LOW.

1.2 AD-CMP-CON/IOCA0

The AD-CMP-CON register defines the pins of port 6 as analog inputs or as digital I/O individually. Table 8 shows the description of the AD-CMP-CON bits

Table 8 The description of AD-CMP-CON bits: I/O configuration

BIT	7	6	5	4	3	2	1	0
SYMBOL	VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0
*Init_Value	0	0	0	0	0	0	0	0

*Init_Value: initial value at power-on reset

VREFS (bit 7): The input source of the Vref of the ADC.

0 = The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53.
1 = The Vref of the ADC is connected to P53/VREF.

CE (bit 6): Control bit used to enable comparator.

0 = Disable comparator.
1 = Enable comparator.

COE (bit 5): Set P57 as the output of the comparator

0 = the comparator acts as an OP if CE=0.
1 = act as a comparator if CE=1.

IMS2~IMS0 (bit 4 ~ bit 2): ADC configuration definition bit. See Table 3.

CKR1 and CKR0 (bit 1 and bit 0): The conversion time select.

00 = Fosc/4;
01 = Fosc/16;
10 = Fosc/64;
11 = Frc (Internal RC clock osc);

1.3 GCON/IOC90

As shown in Fig. 11, OP1 and OP2, the gain amplifiers, are located in the middle of the analog input pins (ADC1 and ADC5) and the 8-1analog switch. The GCON register controls the gains. Table 9 shows the gains and the operating range of ADC.

Table 9 The gains and the operating range of ADC

G10~G12/G40~G42	Gain	Range of Operating Voltage
000	1	VDS ~ (Vref-VDS)
001	2	VDS/2 ~ (1/2) (Vref-VDS)
010	4	VDS/4 ~ (1/4) (Vref-VDS)
011	8	VDS/8 ~ (1/8) (Vref-VDS)
100	16	VDS/16 ~ (1/16) (Vref-VDS)
101	32	VDS/32 ~ (1/32) (Vref-VDS)

<Note> 1. Vref can not be less than 3 volts.
2. VDS can not be less than 0.3 volts.

2. ADC Data Register (ADDATA/RA)

When the A/D conversion is complete, the result is loaded to the ADDATA. The START//END bit is clear, and the ADIF is set.

3. A/D Sampling Time

The accuracy, linearity and speed of the successive approximation A/D converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance affect directly the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 1μs for each kΩ of the analog sources impedance and at least 1μs for the low-impedance source. After the analog input channel is selected, this acquisition time must be done before the conversion can be started.

4. A/D Conversion Time

CKR0 and CKR1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without scarifying the accuracy of A/D conversion. For the EM78P458, the conversion time per bit is about 2μs. Table 10 shows the relationship of Tct and the maximum operating frequencies.

Table 10 Tct vs. the maximum operation frequency

CKR0~CKR1	Operation Mode	Max. Operation Frequency
00	Fosc/4	1 MHz
01	Fosc/16	4 MHz
10	Fosc/64	16 MHz
11	Internal RC	1 MHz

5. A/D operation during the sleep mode

In order to lower power consumption, the A/D conversion can operate during sleep mode and must implement the mode of internal RC clock source. As the SLEP instruction is executed, all the operations of the MCU will stop except the A/D conversion. The RUN bit will be cleared and the result will be fed to the ADDATA when the conversion is completed. If the ADIE is enable, the device will wake up. Otherwise, the A/D conversion will be shut off no matter what the ADPD bit is.

6. Programming steps/considerations

6.1 Programming steps

Follow these steps to obtain data from the ADC:

1) Write to the three bits(IMS2~IMS0) on the AD-CMP-CON1 register to define the characteristics of R6: Digital I/O, analog channels and voltage reference pin.
2) Write to the ADCON register to configure AD module:
   a) Select A/D input channel (ADIS2~ADIS0);
   b) Select the proper gains by writing the GCON register (optional);
   c) Define A/D conversion clock rate(CKR1~CKR0);
   d) Set the /ADPD bit to 1 to begin sampling.
3) Put "ENI" instruction, if the interrupt function is employed.
4) Set the ADRUN bit to 1.
5) Wait for either the interrupt flag to be set or the ADC interrupt to occur.
6) Read ADDATA, the conversion data register.
7) Clear the interrupt flag bit (ADIF).
8) For next conversion, go to step 1 or step 2 as required. At least 2 Tct is required before next acquisition starts.

<Note>: To obtain an accurate value, it is necessary to avoid any data transition on I/O pins during AD conversion.

6.2 An example demonstration programs

```
; To define the general registers
R_0     == 0                    ; Indirect addressing register
PSW     == 3                    ; Status register
PORT5   == 5
PORT6   == 6
R_F     == 0XF                  ; Interrupt status register

; To define the control register
IOC50   == 0X5                  ; Control register of Port 5
IOC60   == 0X6                  ; Control register of Port 6
C_INT   == 0XF                  ; Interrupt control register

;ADC control registers
ADDATA      == 0xA              ; The contents are the results of ADC
```

```
ADCONR    == 0x9                ;   7     6     5     4     3     2     1     0
                                ;   -     -   IOCS ADRUN ADPD  ADIS2 ADIS1 ADIS0
ADCONC    == 0xA                ;   7     6     5     4     3     2     1     0
                                ; VREFS   X     X   IMS2  IMS1  IMS0  CKR1  CKR0
GCON  == 0x9                    ;   7     6     5     4     3     2     1     0
                                ; OPE2  OPE1  G22   G21   G20   G12   G11   G10
;To define bits

;In ADCONR
ADRUN     == 0x4                ; ADC is executed as the bit is set
ADPD  == 0x3                    ; Power mode of ADC

          ORG 0                 ; Initial address
          JMP INITIAL           ;
          ORG 0x08              ; Interrupt vector

          (User program)

          CLR R_F               ; To clear the ADCIF bit
          BS ADCONR, ADRUN      ; To start to execute the next AD conversion if necessary
          RETI
INITIAL:
          MOV A, @0bXXXX1XXX    ; Enable the interrupt function of ADC, "X" by application
          IOW C_INT
          MOV A, @0xXX          ; Interrupt disabled:<6>
          CONTW
          MOV A, @0b00000000    ; To employ Vdd as the reference voltage, to define P60 as
          IOW ADCONC            ; an analog input and the clock rate at fosc/4
En_ADC:
     MOV A, @0xXXXXXXX1         ; To define P60 as an input pin, and the others are dependent
     IOW PORT6                  ; on applications
     MOV A, @0b01000111         ; To enable the OP1, and set the gain to be 32
     IOW GCON
     BS ADCONR, ADPD            ; To disable the power-down mode of ADC
     ENI                        ; Enable the interrupt function
     BS ADCONR, ADRUN           ; To start to run the ADC
; If the interrupt function is employed, the following three lines may be ignored
POLLING:
     JBC ADCONR, ADRUN          ; To check the ADRUN bit continuously;
     JMP POLLING                ; it will reset as the AD conversion completed
     (User program)
     :
     :
     :
```

VI.8 Dual sets of PWM (Pulse Width Modulation)

1. Overview

In PWM mode, both pins of PWM1 and PWM2 produce up to a 10-bit resolution PWM output. Fig. 12 shows the functional block diagram. A PWM output has a period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the period. Fig. 13 depicts the relationships between a period and a duty cycle.

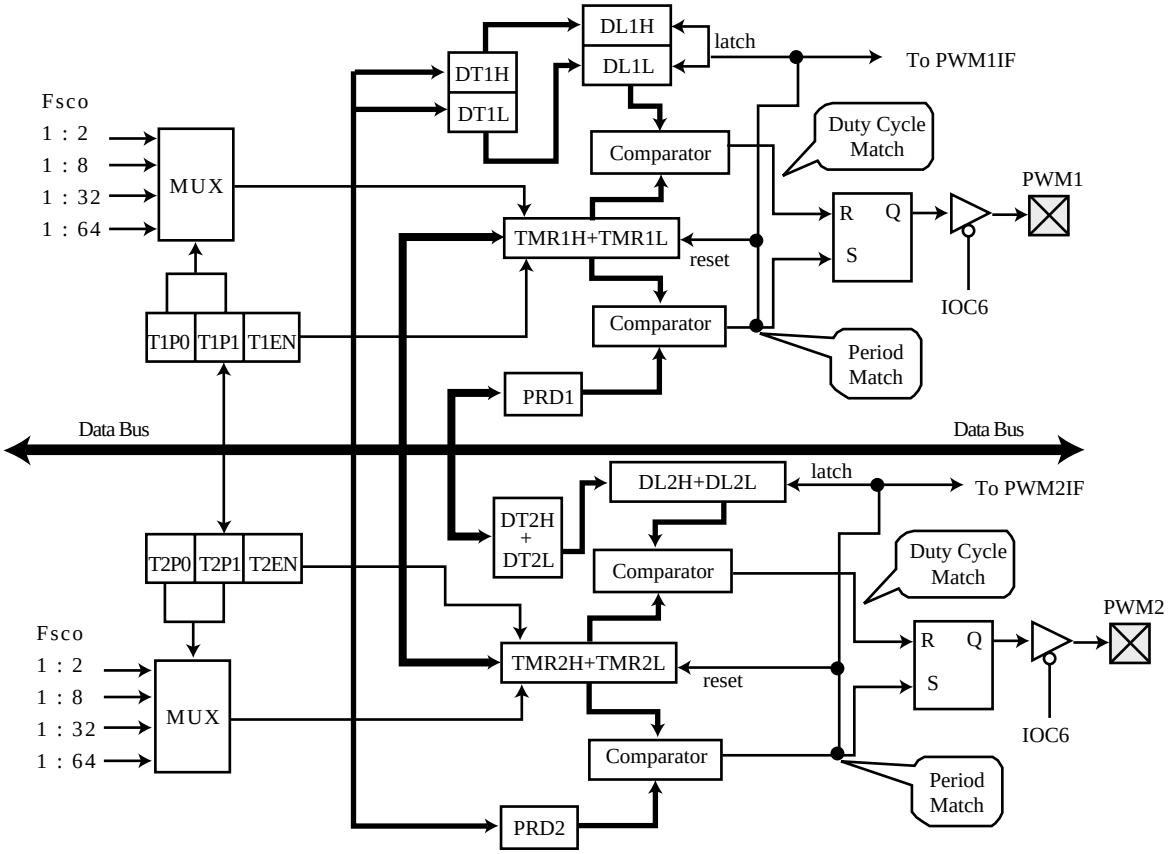


Fig. 12 The functional block diagram of the dual PWMs

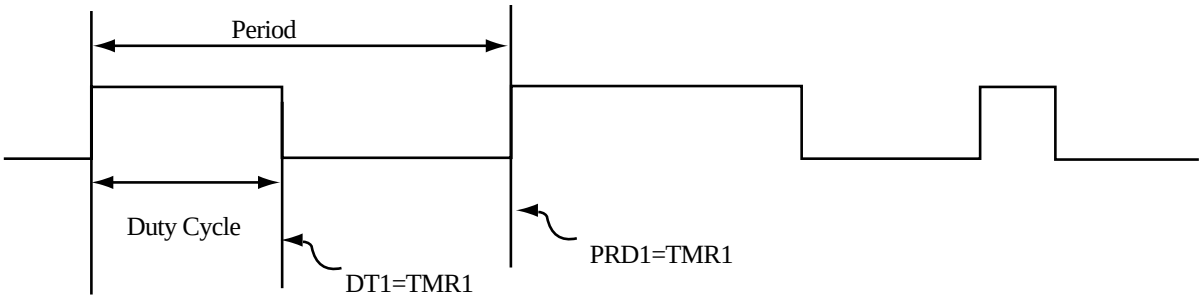


Fig. 13 The output timing of the PWM

2. Increment Timer Counter (TMRX: TMR1H/TWR1L or TMR2H/TWR2L)

TMRX are ten-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written and cleared on any reset conditions. If employed, they can be turned down for power saving by setting T1EN bit [PWMCON<4>] or T2EN bit [PWMCON<5>] to 0.

3. PWM Period (PRDX : PRD1 or PRD2)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared.
- The PWMX pin is set to 1.
- The PWM duty cycle is latched from DT1/DT2 to DTL1/DTL2.
  < Note > The PWM output will not be set, if the duty cycle is 0.
- The PWMXIF pin is set to 1.

The following formula describes how to calculate the PWM period:

PERIOD = (PRDX + 1) * 4 * (1/Fosc) * (TMRX prescale value)

4. PWM Duty Cycle (DTX: DT1H/ DT1L and DT2H/ DT2L; DTL: DL1H/DL1L and DL2H/DL2L)

The PWM duty cycle is defined by writing to the DTX register and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it can not be latched into DTL until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

Duty Cycle = (DTX) * (1/Fosc) * (TMRX prescale value)

5. ComparatorX

To change the output status while the match occurs, the TMRXIF flag will be set at the same time.

6. PWM programming procedures/steps

(1) Load PRDX with the PWM period.
(2) Load DTX with the PWM Duty Cycle.
(3) Enable interrupt function by writing IOCF0, if required.
(4) Set PWMX pin to be output by writing a desired value to IOC60.
(5) Load a desired value to IOC51 with TMRX prescaler value and enable both PWMX and TMRX.

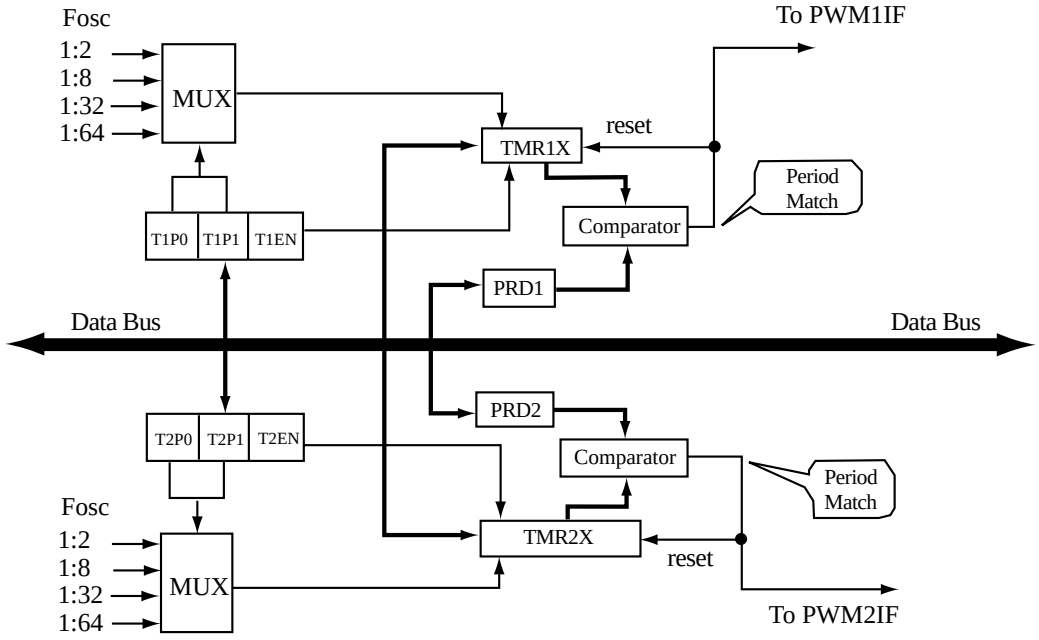
VI.9 Timer

1. Overview

Timer1 (TMR1) and Timer2 (TMR2) (TMRX) are 10-bit clock counters with programmable prescalers, respectively. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written and cleared on any reset conditions.

2. Function description

Fig. 14 shows TMRX block diagram. Each signal and block are described as follows:



*TMR1X=TMR1H+TMR1L.
*TMR2X=TMR2H+TMR2L.

Fig. 14 TIMERX block diagram

Fosc: Input clock.
Prescaler (T1P0 and T1P1/T2P1 and T2P0): Options of 1:2, 1:8, 1:32 and 1:64 are defined by CLKX. It is cleared while a value is written to TMRX, PWMCON or any kind of reset.

TMR1X and TMR2X (TMR1H/TWR1L and TMR2H/TMR2L): Timer X register; TMRX is increased until it matches with PRDX, and then is reset to 0. TMRX cannot be read.

PRDX (PRD1 and PRD2): PWM period register.

ComparatorX (Comparator 1 and Comparator 2): To reset TMRX while the match occurs and the TMRXIF flag will be set at the same time.

3. Programming the related registers

As the TMRX is defined, the related registers of this operation are shown in Table 11.It must be aware that the PWMX bits must be disabled if their related TMRXs are employed. That is, bit 7 and bit 6 of the PWMCON register must be set to '0'.

Table 11 Related control registers of TMR1 and TMR2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC51	PWMCON/IOC51	PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

4. Timer programming procedures/steps

(1) Load PRDX with the TIMER period.
(2) Enable interrupt function by writing IOCF0, if required
(3) Load a desired value to PWMCON with the TMRX prescaler value and enable both TMRX and disable PWMX.

VI.10 Comparator

EM78P458/9 has one comparator, which has two analog inputs and one output. The comparator can be employed to wake up from the sleep mode. Fig. 15 shows the circuit of the comparator.

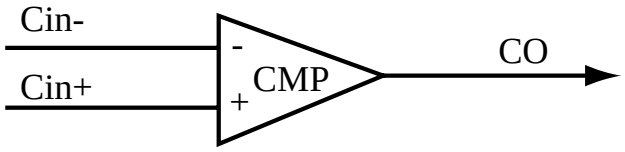


Fig. 15 Comparator operating mode

1. External reference signal

The analog signal that is presented at Cin- compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly.

- The reference signal must be between Vss and Vdd.
- The reference voltage can be applied to either pin of comparator.
- Threshold detector applications may be the same reference.
- The comparator can operate from the same or different reference source.

2. Comparator outputs

- The compared result is stored in the CMPOUT of R3.
- The comparator outputs can output to P57 by programming bit5<COE> of the AD-CMPCON register to 1.
- P57 must be defined as output if implemented as the comparator output.
- Fig. 16 shows the comparator output block diagram.

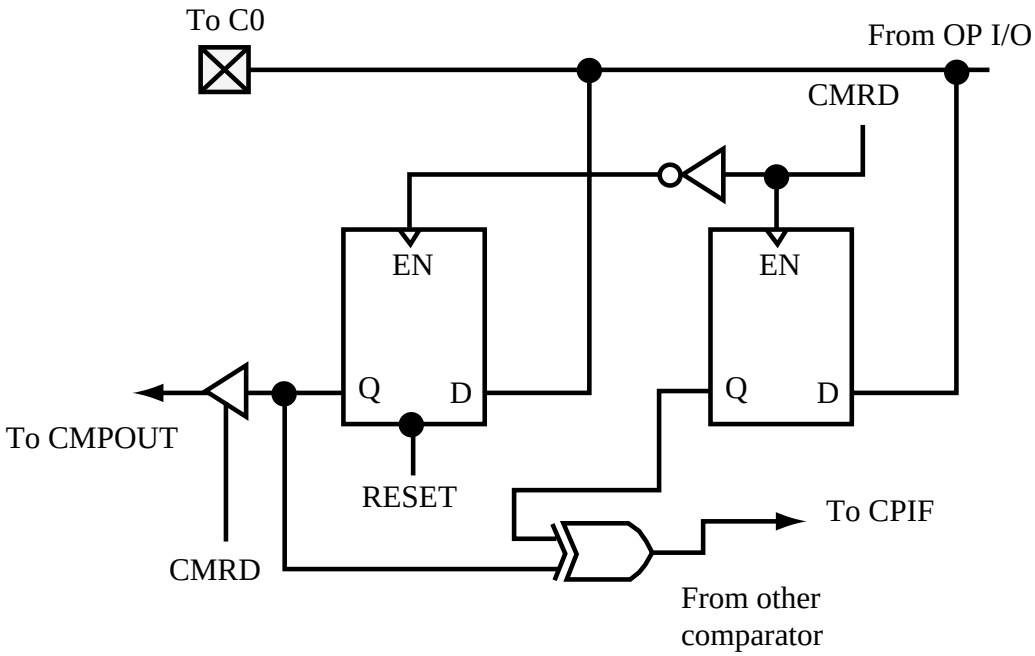


Fig. 16 The output configuration of a comparator

3. Using as an operation amplifier

The comparator can be used as an operation amplifier, if a feedback resister is connected from the input to the output externally. In this case, the Schmitt trigger can be disabled for power saving by setting CE to 1 and COE to 0.

4. Interrupt

- INTE(CONT.7) and CMPIE(IOCF0.6) must be enabled.
- Interrupt occurs whenever changes occur on the output pin of the comparator.
- The actual change on the pin can be determined by reading bit CMPOUT, R3<7>.
- CMPIF(RF.6), the comparator interrupt flag, can only be cleared by software.
- The difference of the inputs of the comparator will continue to set the CMPIF bit.

5. Wake-up from the SLEEP mode

- If enabled, the comparator remains active and the interrupt is still functional, even in the SLEEP mode.
- If a mismatch occurs, the interrupt will wake up the device from SLEEP mode.
- The power consumption should be taken into consideration due to the issue of the power saving.
- If the function is unemployed during SLEEP mode, turn off comparator before entering sleep mode.

VI.11 The initialized values after reset

Table 12 The summary of the initialized values for registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCB0	Bit Name	/PD7	/PD6	*/PD5	*/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCC0	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCD0	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCE0	Bit Name	WDTE	EIS	X	X	X	X	X	X
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	1	1	1	1	1	1
N/A	IOCF0	Bit Name	X	CMPE	PMW21E	PWM11E	ADIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	P	P	P	P	P	P	P
N/A	IOC90 (GCON)	Bit Name	OP2E	OP1E	G42	G41	G40	G12	G11	G10
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCA0 (AD-CMP CON)	Bit Name	VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P

Preliminary

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC51 (PWMCON)	Bit Name	PWM2E	PWM2E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC61 (DT1L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	p	p	p	p	p	p	p	p
N/A	IOC71 (DT1H)	Bit Name	CALI1	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	X	Bit1	Bit0
		Power-on	0	1	1	0	0	0	0	0
		/RESET and WDT	0	1	1	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC81 (PRD1)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC91 (DT2L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCA1 (DT2H)	Bit Name	CALI2	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	X	Bit1	Bit0
		Power-on	0	1	1	0	0	0	0	0
		/RESET and WDT	0	1	1	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCB1 (PRD2)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	p	p	p	p	p	p	p	p
N/A	IOCC1 (DL1L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCD1 (DL1H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
N/A	IOCE1 (DL2L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	p	p	p	p	p	p	p	p
N/A	IOCF1 (DL2H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	p	p
N/A	CONT	Bit Name	/INTE	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Changed	p	p	p	p	p	p	p	p

Preliminary

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	p	p	p	p	p	p	p	p
0X02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	Jump to address 0x08 or continue to execute next instruction							
0x03	R3(SR)	Bit Name	GP2	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Changed	p	p	p	t	t	P	P	P
0x04	R4(RSR)	Bit Name	BS7	BS6	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x05	P5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x07~0x8	R7~R8	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x9	R9 (ADCON)	Bit Name	X	X	IOCS	ADRUN	ADPD	ADAS2	ADAS1	ADAS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0xA	RA (ADDATA)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0xB	RB (TMR1L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0xC	RC (TMR1H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	p	p

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xD	RD (TMR2L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0xE	RE (TMR2H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	p	p
0xF	RF (ISR)	Bit Name	X	CMPIF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	p	p	p	p	p	p	p
0x10~0x3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	p	p	p	p	p	p	p	p
		Wake-up from Pin Changed	p	p	p	p	p	p	p	p

X : not used. U: unknown or don't care. P : previous value before reset.

VI.12 Oscillator

1. Oscillator Modes

The EM78P458 and EM78P459 can be operated in four different oscillator modes which are Internal RC oscillator mode (IRC), External RC oscillator mode(ERC), High XTAL oscillator mode(HXT) and Low XTAL oscillator mode(LXT). Users can select one of them by programming the MASK option.

2. Crystal Oscillator/Ceramic Resonators (XTAL)

EM78P458/9 can be driven by an external clock signal through the OSCI pin as shown in Fig. 17.

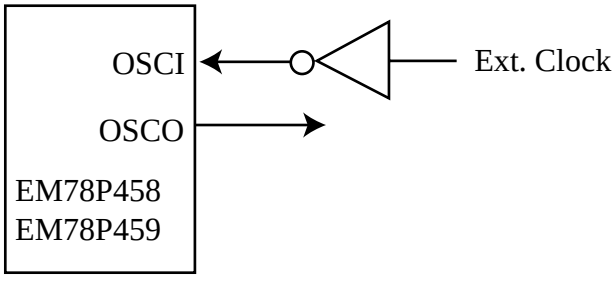


Fig. 17 Circuit for External Clock Input

In the most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 18 depicts the circuit. It is the same no matter in the HXT mode or in the LXT mode. Table 17 recommends the values of C1 and C2. Since each resonator has its own attribute, users should refer to their specifications for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

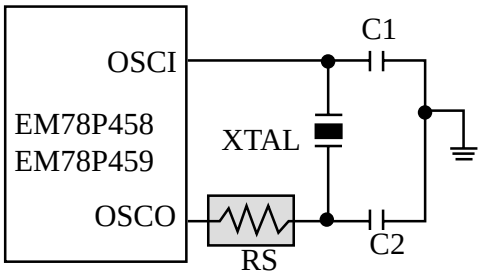


Fig. 18 Circuit for Crystal/Resonator

Table 13 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonator	HXT	455KHz	100~150	100~150
		2.0MHz	20~40	20~40
		4.0MHz	10~30	10~30
Crystal Oscillator	LXT	32.768KHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

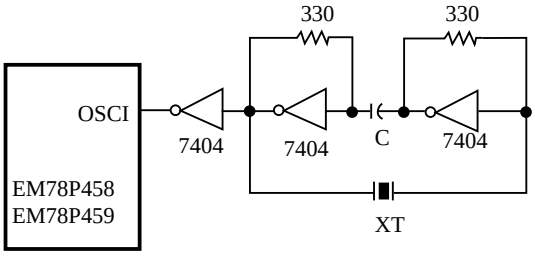


Fig. 19 Circuit for Crystal/Resonator (Series Mode)

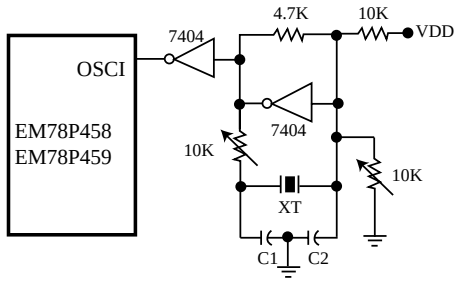


Fig. 20 Circuit for Crystal/Resonator (Parallel Mode)

3. External RC Oscillator Mode

For some applications whose timing need not be calculated precisely, the RC oscillator (Fig. 21) offers a lot of cost savings. Nevertheless, it should be aware that the frequency of the RC oscillator is the function of the supply voltage, the values of the resistor (Rext), the capacitor(Cext) and even the operation temperature. Moreover to this, the frequency also changes slightly from one chip to another due to the process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF as well as the value of Rext should not be greater than 1M ohm. If they can not be kept in this range, the frequency is affected easily by noise, humidity and leakage.

The smaller Rext the RC oscillator has, the faster frequency it gets. On the contrary, for very low Rext values, for instance, 1KΩ, the oscillator becomes unstable because the NMOS can not discharge the current of the capacitance correctly.

On a basis of above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types and the ways of PCB layout will effect the system frequency.

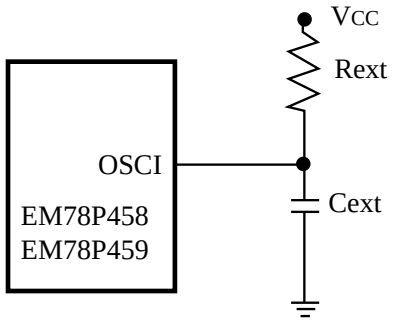


Fig. 21 Circuit for External RC Oscillator Mode

Table 14 RC Oscillator Frequencies

Cext	Rext	Average Fosc @ 5V, 25°C	Average Fosc @ 3V, 25°C
20 pF	3.3k	1.13 MHz	974 KHz
	5.1k	2.22 MHz	1.83 MHz
	10k	1.28 MHz	1.14 MHz
	100k	150 KHz	143 KHz
100 pF	3.3k	1.13 MHz	974 KHz
	5.1k	758 KHz	675 KHz
	10k	409 KHz	376 KHz
	100k	51 KHz	43.7 KHz
300 pF	3.3k	472 KHz	420 KHz
	5.1k	310 KHz	283 KHz
	10k	165 KHz	153 KHz
	100k	17.5 KHz	17.0 KHz

<Note> 1. Measured on DIP packages.
2. Design reference only

VI.13 Power-on Considerations

Any microcontroller is not warranted to start proper operation before the power supply stays in its steady state.

EM78P458/9 is equipped with Power On Voltage Detector (POVD) whose detective level is from 1.4 V to 2.0 V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

1. External Power-on Reset Circuit

The circuit shown in Fig. 22 implements an external RC to produce the reset pulse. The pulse width (time constant) should keep long enough until Vdd has reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40 K. In this way, the voltage in pin /RESET will be held below 0.2V. The diode (D) acts a short circuit at the moment of power-down. The capacitor, C, will be discharged rapidly and fully. Rin, the current-limited resistor, protects against a high discharging current or ESD(electrostatic discharge) flowing to pin /RESET.

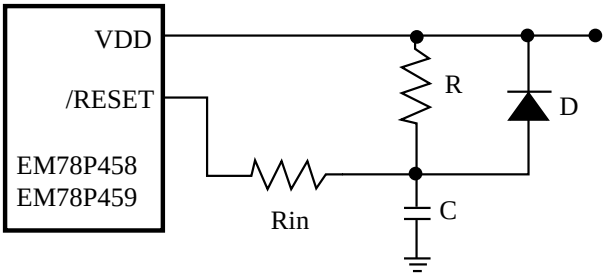


Fig. 22 External Power-up Reset Circuit

2. Residue Voltage Protection

In some applications, replacing battery as an instance, device power (Vdd) is taken off and recovered within a few seconds. A residue voltage which trips below Vdd min but not to zero may exist. This condition may cause a poor power-on reset. Fig. 23 and Fig. 24 show how to build the residue voltage protection circuit

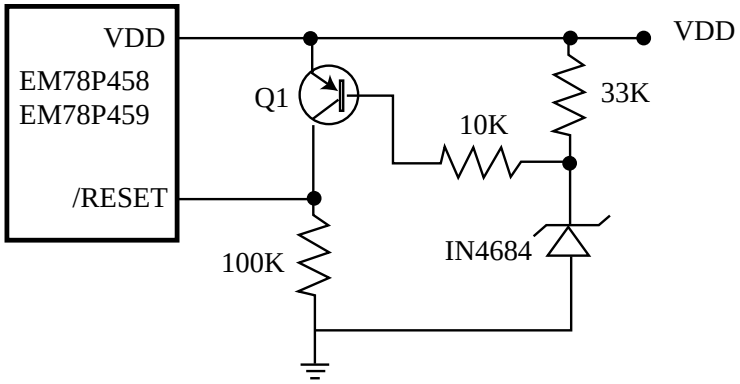


Fig. 23 Circuit 1 for the residue voltage protection

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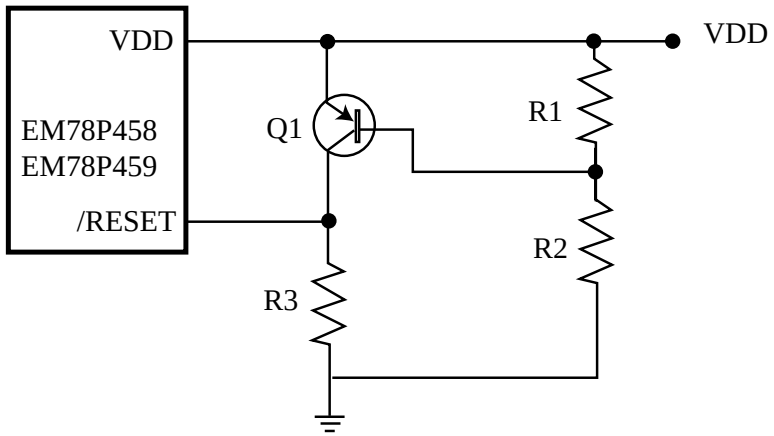

Fig. 24 Circuit 2 for the residue voltage protection

VI.14 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction “MOV R2,A”, “ADD R2,A” or instructions of arithmetic or logic operation on R2 (e.g. “SUB R2,A”, “BS(C) R2,6”, “CLR R2”, ...). In this case, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared or tested directly.
(2) The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

The symbol “R” represents a register designator which specifies which one of the registers (including operational registers and general-purpose registers) to be utilized by the instruction. The symbol “b” represents a bit field designator which selects the number of the bit located in the register “R” affected by the operation. The symbol “k” represents an 8 or 10-bit constant or literal value.

Table 15 The list of the instruction set of EM78P458 and EM78P459

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A→CONT	None
0 0000 0000 0011	0003	SLEP	0→WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0→WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A→IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack]→PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack]→PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT→A	None
0 0000 0001 rrrr	001r	IOR R	IOCR→A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A→R2 Bits 8~9 of R2 unchanged	 Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A→R	None
0 0000 1000 0000	0080	CLRA	0→A	Z
0 0000 11rr rrrr	00rr	CLR R	0→R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A→A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A→R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1→A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1→R	Z
0 0010 00rr rrrr	02rr	OR A,R	A∨VR→A	Z
0 0010 01rr rrrr	02rr	OR R,A	A∨VR→R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R→A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R→R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R→A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R→R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R→A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R→R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R→A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R→R	Z
0 0100 10rr rrrr	04rr	COMA R	/R→A	Z
0 0100 11rr rrrr	04rr	COM R	/R→R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1→A	Z
0 0101 01rr rrrr	05rr	INC R	R+1→R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1→A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1→R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n)→A(n-1) R(0)→C, C→A(7)	 C
0 0110 01rr rrrr	06rr	RRC R	R(n)→R(n-1) R(0)→C, C→R(7)	 C
0 0110 10rr rrrr	06rr	RLCA R	R(n)→A(n+1) R(7)→C, C→A(0)	 C
0 0110 11rr rrrr	06rr	RLC R	R(n)→R(n+1) R(7)→C, C→R(0)	 C

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INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3)→A(4-7) R(4-7)→A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3)↔R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1→A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1→R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0→R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1→R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1→[SP] (Page, k) →PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k)→PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k →A	None
1 1001 kkkk kkkk	19kk	OR A,k	A∨ k→A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k→A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕k→A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k→A, [Top of Stack]→PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A→A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1→[SP], 001H→PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A→A	Z,C,DC

<Note1> This instruction can operate on IOC50 ~ IOC60, IOC90~IOCF0, IOC51~IOCF1 only.
<Note2> This instruction is not recommended to operate on RF.
<Note3> This instruction cannot operate on RF.

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VII. ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

VIII. DC ELECTRICAL CHARACTERISTIC (Ta=0°C ~ 70°C, V_{DD}=5.0V±5%, V_{SS}=0V)

Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
XTAL : VDD to 3V	Fxt	Two cycles with two clocks	DC		4.0	MHz
XTAL : VDD to 5V			DC		16.0	MHz
RC : VDD to 5V	F_{RC}	R : 5.0KΩ , C : 39pF	F_{RC}±20%	602	F_{RC}±20%	KHz
Input Leakage Current for input pins	I_{IL}	V_{IN} = V_{DD}, V_{SS}			±1	µA
Input High Voltage	V_{IH}	Port 5,6	1.8			V
Input Low Voltage	V_{IL}	Port 5,6			0.8	V
Input High Threshold Voltage	V_{IHT}	/RESET, TCC	2.0			V
Input Low Threshold Voltage	V_{ILT}	/RESET, TCC			0.8	V
Clock Input High Voltage	V_{IHX}	OSCI	2.5			V
Clock Input Low Voltage	V_{ILX}	OSCI			1.0	V
Output High Voltage (Port 5,6)	V_{OH1}	I_{OH} = -12.0mA	2.4			V
Output Low Voltage (P50~P53 P60~P63, P66~P67)	V_{OL1}	I_{OL} = 12.0mA			0.4	V
Output Low Voltage (P64,P65)	V_{OL2}	I_{OL} = 16.0mA			0.4	V
Pull-high current	I_{PH}	Pull-high active, input pin at V_{SS}	-50	-100	-240	µA
Pull-down current	I_{PD}	Pull-down active, input pin at V_{DD}	25	50	120	µA
Power-down current	I_{SB}	All input and I/O pins at V_{DD}, output pin floating, WDT enabled			4	µA
Power-down current	I_{SB}	All input and I/O pins at V_{DD}, output pin floating, WDT disabled			0.2	µA
Operating supply current (V_{DD}=3V) at two cycles/two clocks	I_{CC1}	/RESET='High', Fosc=32KHz(Crystal type, CLKS="0"), output pin floating, WDT disabled	15	15	30	µA
Operating supply current (V_{DD}=3V) at two cycles/two clocks	I_{CC2}	/RESET='High', Fosc=32KHz(Crystal type,CLKS="0"), output pin floating, WDT enabled		19	35	µA
Operating supply current (VDD=5V) at two cycles/two clocks	I_{CC3}	/RESET='High', Fosc=2MHz (Crystal type,CLKS="0"), output pin floating			1.3	mA
Operating supply current (VDD=5V) at two cycles/two clocks	I_{CC4}	/RESET='High', Fosc=4MHz (Crystal type,CLKS="0"), output pin floating			4.0	mA

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IX. VOLTAGE DETECTOR ELECTRICAL CHARACTERISTIC (Ta= 25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	Vdet		1.8	2.0	2.2	V
Release voltage	Vrel			Vdet x1.05		V
Current consumption	Iss	V_{DD} = 5V			5	μA
Operating voltage	Vop		0.7*		5.5	V
Temperature characteristic of Vdet	ΔVdet/ ΔTa	0°C ≤Ta≤ 70°C			-2	mV/°C

* When the voltage of V_{DD} rises between Vop=0.7V and Vdet, the output of voltage detector must be "Low".

X. AC ELECTRICAL CHARACTERISTICS (Ta=0°C ~ 70°C, V_{DD}=5.0V±5%, V_{SS}=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time (CLKS="0")	Tins	XTAL Type	125		DC	ns
		RC Type	500		DC	ns
TCC input period	Ttcc		(Tins+20)/N*			ns
Device reset hold time	Tdrh	Ta = 25°C	9	18	30	ms
/RESET pulse width	Trst	Ta = 25°C	2000			ns
Watchdog Timer period	Twdt	Ta = 25°C	9	18	30	ms
Input pin setup time	Tset			0		ns
Input pin hold time	Thold			20		ns
Output pin delay time	Tdelay	Cload=20pF		50		ns

Note : N*= selected prescaler ratio.