

## CMOS Hex Buffer

High-Voltage Types (20-Volt Rating)

3-State Non-Inverting Type

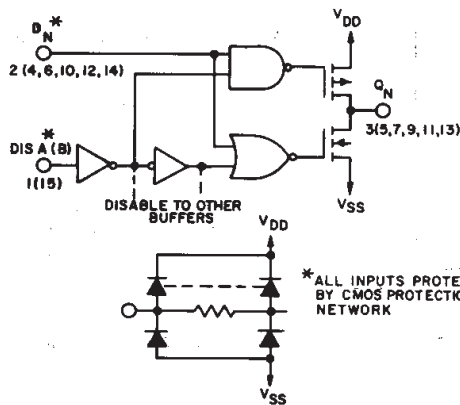
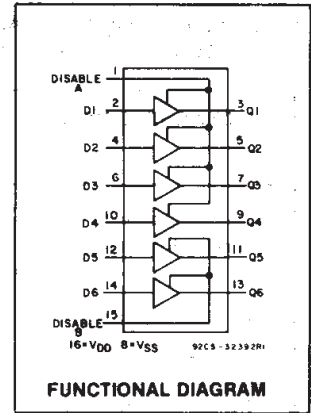
■ CD4503B is a hex noninverting buffer with 3-state outputs having high sink- and source-current capability. Two disable controls are provided, one of which controls four buffers and the other controls the remaining two buffers. The CD4503B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

### Features:

- 1 TTL-load output drive capability
- 2 output-disable controls
- 3-state outputs
- Pin compatible with industry types MM80C97, MC14503, and 340097
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- 3-state hex buffer for interfacing IC's with data buses
- CMOS to TTL hex buffer



TRUTH TABLE

D <sub>N</sub>	DISA(B)	Q <sub>N</sub>
0	0	0
1	0	1
X	1	HIGH Z

X = DON'T CARE

92CM-32393

Fig. 1—Logic diagram of 1 to 6 identical buffers.

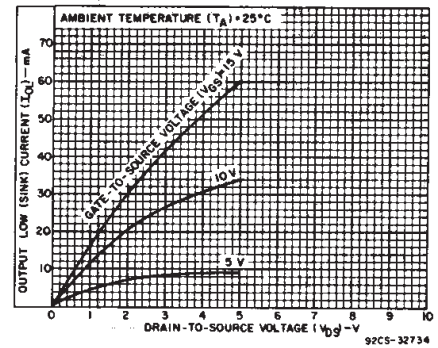


Fig. 2—Typical n-channel output low (sink) current characteristics.

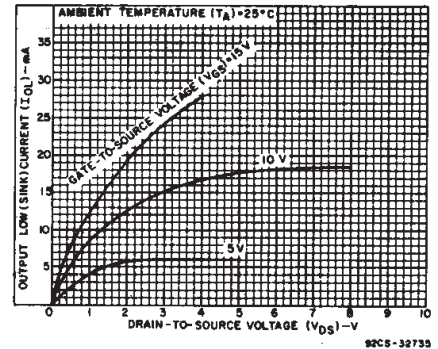


Fig. 3—Minimum n-channel output low (sink) current characteristics.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)

Voltages referenced to V<sub>SS</sub> Terminal ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub> +0.5V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm$ 10mA

POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

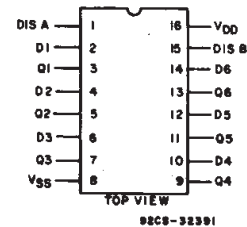
FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C

STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max ..... +265°C



92CS-32391

### TERMINAL ASSIGNMENT

# CD4503B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	1	1	30	30	—	0,02	1	μA
	—	0,10	10	2	2	60	60	—	0,02	2	
	—	0,15	15	4	4	120	120	—	0,02	4	μA
	—	0,20	20	20	20	600	600	—	0,04	20	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0,4	0	5	2,6	2,5	1,4	1,3	2,1	2,3	—	mA
	0,5	0	10	6,5	6,4	3,9	3,8	5,5	6,2	—	
	1,5	0	15	19,2	18,9	11,4	11,2	16,1	23	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4,6	5	5	-1,2	-1,16	-0,7	-0,7	-1,02	-1,9	—	mA
	2,5	5	5	-5,8	-5,7	-3,4	-3	-4,8	-6,1	—	
	9,5	10	10	-3,1	-3	-1,9	-1,8	-2,6	-3,7	—	
	13,5	15	15	-8,2	-8	-4,9	-4,8	-6,8	-14,1	—	V
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0,05				—	0	0,05	
	—	0,10	10	0,05				—	0	0,05	
	—	0,15	15	0,05				—	0	0,05	V
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4,95				4,95	5	—	
	—	0,10	10	9,95				9,95	10	—	
	—	0,15	15	14,95				14,95	15	—	V
Input Low Voltage, V <sub>IL</sub> Max.	0,5,4,5	—	5	1,5				—	—	1,5	
	1,9	—	10	3				—	—	3	
	1,5,13,5	—	15	4				—	—	4	V
Input High Voltage, V <sub>IH</sub> Min.	0,5,4,5	—	5	3,5				3,5	—	—	
	1,9	—	10	7				7	—	—	
	1,5,13,5	—	15	11				11	—	—	μA
Input Current I <sub>IN</sub> Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 <sup>-5</sup>	±0,1	
3-State Output Leakage Current, I <sub>OUT</sub> Max.	0,18	0,18	18	±0,4	±0,4	±12	±12	—	±10 <sup>-4</sup>	±0,4	

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)	3	18	V

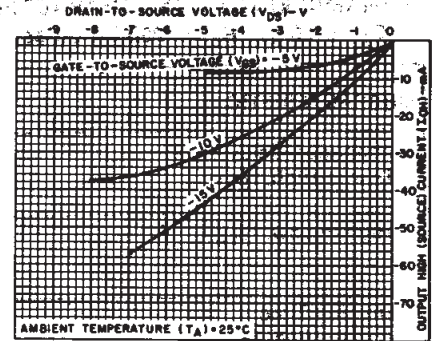


Fig. 4—Typical p-channel output high (source) current characteristics.

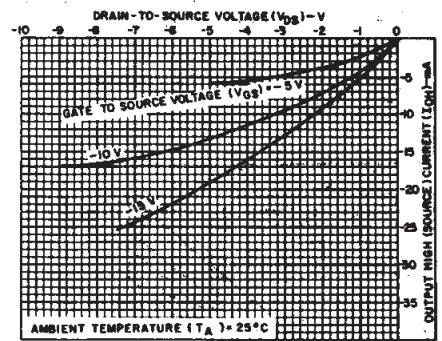


Fig. 5—Minimum p-channel output high (source) current characteristics.

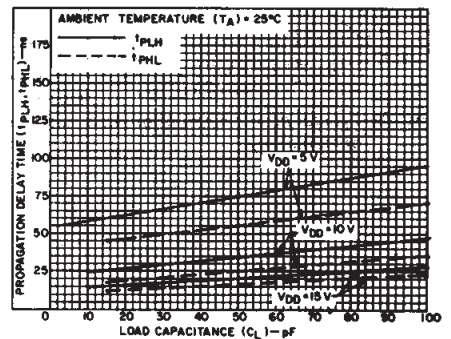


Fig. 6—Typical propagation delay time as a function of load capacitance.

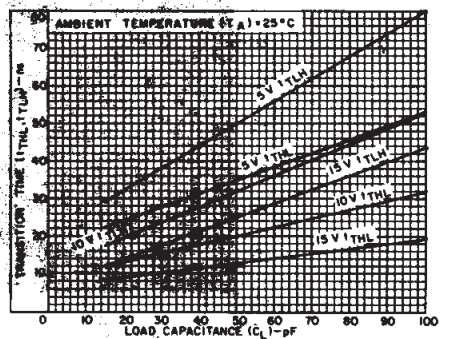


Fig. 7—Typical transition time as a function of load capacitance.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4503B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$  unless otherwise specified.**

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		Typ.	Max.	
Propagation Delay Time: Low-to-High, $t_{PLH}$	5	75	150	ns
	10	35	70	
	15	25	50	
High-to-Low, $t_{PHL}$	5	55	110	ns
	10	25	50	
	15	17	35	
Transition Time: Low-to-High, $t_{TLH}$	5	50	90	ns
	10	30	45	
	15	25	35	
High-to-Low, $t_{THL}$	5	35	70	ns
	10	20	40	
	15	13	25	
3-State Propagation Delay Time: $R_L = 1\text{ k}\Omega$ $t_{PHZ}, t_{PZH}$	5	70	140	ns
	10	30	60	
	15	25	50	
$t_{PZL}, t_{PLZ}$	5	90	180	ns
	10	40	80	
	15	35	70	

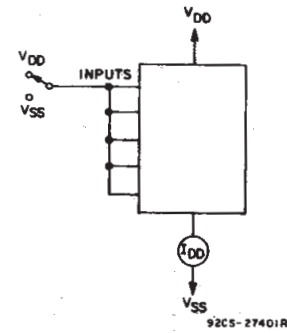


Fig. 10—Quiescent device current test circuit.

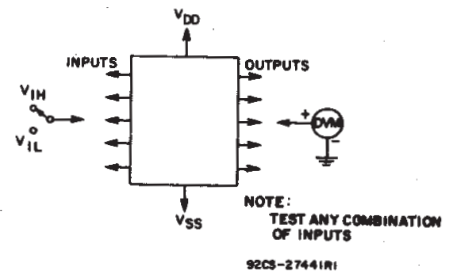


Fig. 11—Input voltage test circuit.

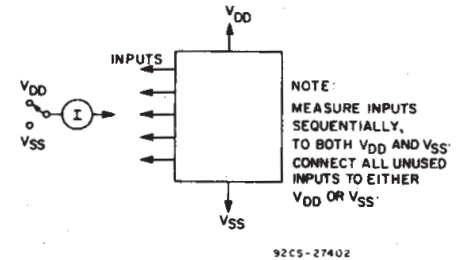


Fig. 12—Input current test circuit.

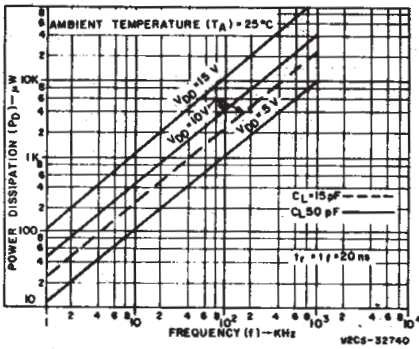


Fig. 8—Typical power dissipation as a function of frequency.

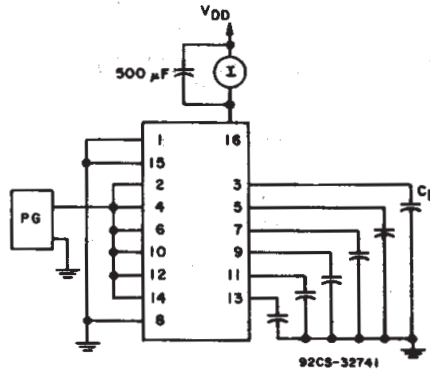
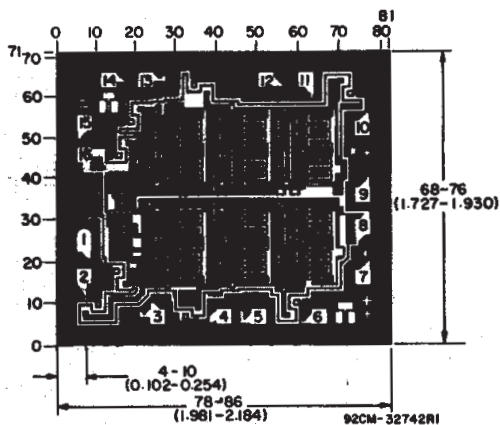


Fig. 9—Dynamic power dissipation test circuit.



## Dimensions and pad layout for CD4503BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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