1 GSPS Direct Digital Synthesizer

AD9858

FEATURES

1 GSPS internal clock speed
Up to 2 GHz input clock (selectable divide-by-2)
Integrated 10-bit D/A converter
Phase noise < 145 dBc/Hz @ 1 kHz offset
Output frequency = 100 MHz (DAC output)
32-bit programmable frequency register
Simplified 8-bit parallel and SPI® serial control interface
Automatic frequency sweeping capability
4 frequency profiles
3.3 V power supply
Power dissipation 2 W typical
Integrated programmable charge pump and phase frequency detector with fast lock circuit
Isolated charge pump supply up to 5 V
Integrated 2 GHz mixer

APPLICATIONS

VHF/UHF LO synthesis
Tuners
Instrumentation
Agile clock synthesis
Cellular base station hopping synthesizer
Radar
Sonet/SDH clock synthesis

GENERAL DESCRIPTION

The AD9858 is a direct digital synthesizer (DDS) featuring a 10-bit DAC operating up to 1GSPS. The AD9858 uses advanced DDS technology, coupled with an internal high speed, high performance D/A converter to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sine wave at up to 400+ MHz. The AD9858 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9858 via parallel (8-bit) or serial loading formats. The AD9858 contains an integrated charge pump (CP) and phase frequency detector (PFD) for synthesis applications requiring the combination of a high speed DDS along with phase-locked loop (PLL) functions. An analog mixer is also provided on-chip for applications requiring the combination of a DDS, PLL, and mixer, such as frequency translation loops, tuners, and so on. The AD9858 also features a divide-by-2 on the clock input, allowing the external clock to be as high as 2 GHz.

The AD9858 is specified to operate over the extended industrial temperature range of –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

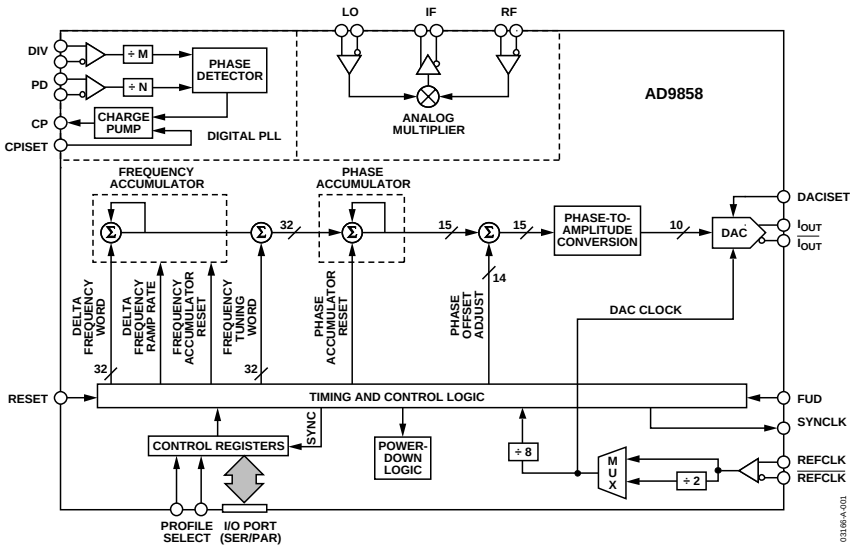

Figure 1.

Rev. A

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AD9858—ELECTRICAL SPECIFICATIONS

Table 1. Unless otherwise noted, V_{DD} = 3.3 V ± 5%, CPV_{DD} = 5 V ± 5%, R_{SET} = 2 kΩ, C_{PISET} = 2.4 kΩ, Reference Clock Frequency = 1 GHz.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
REF CLOCK INPUT CHARACTERISTICS[1, 2]						
Reference Clock Frequency Range (Divider Off)	Full	VI	10		1000	MHz
Reference Clock Frequency Range (Divider On)	Full	VI	20		2000	MHz
Duty Cycle @ 1 GHz	25°C	V	42	50	58	%
Input Capacitance	25°C	V		3		pF
Input Impedance	25°C	IV		1500		Ω
Input Sensitivity	Full	VI	–20		+5	dBm
DAC OUTPUT CHARACTERISTICS						
Resolution	Full			10		Bits
Full-Scale Output Current	Full		5	20	40	mA
Gain Error	Full	VI	–10		+10	% FS
Output Offset	Full	VI			15	µA
Differential Nonlinearity	Full	VI		0.5	1	LSB
Integral Nonlinearity	Full	VI		1	1.5	LSB
Output Impedance	Full	VI		100		kΩ
Voltage Compliance Range	Full	VI	AV_{DD} – 1.5		AV_{DD} + 0.5	V
Wideband SFDR (DC to Nyquist)						
40 MHz F_{OUT}	Full	V		60		dBc
100 MHz F_{OUT}	Full	V		54		dBc
180 MHz F_{OUT}	Full	V		53		dBc
360 MHz F_{OUT}	Full	V		50		dBc
180 MHz F_{OUT} (700 MHz REFCLK)	Full	IV	52			dBc
Narrow-Band SFDR[3]						
40 MHz F_{OUT} (±15 MHz)	Full	V		82		dBc
40 MHz F_{OUT} (±1 MHz)	Full	V		87		dBc
40 MHz F_{OUT} (±50 kHz)	Full	V		88		dBc
100 MHz F_{OUT} (±15 MHz)	Full	V		81		dBc
100 MHz F_{OUT} (±1 MHz)	Full	V		82		dBc
100 MHz F_{OUT} (±50 kHz)	Full	V		86		dBc
180 MHz F_{OUT} (±15 MHz)	Full	V		74		dBc
180 MHz F_{OUT} (±1 MHz)	Full	V		84		dBc
180 MHz F_{OUT} (±50 kHz)	Full	V		85		dBc
360 MHz F_{OUT} (±15 MHz)	Full	V		75		dBc
360 MHz F_{OUT} (±1 MHz)	Full	V		85		dBc
360 MHz F_{OUT} (±50 kHz)	Full	V		86		dBc
180 MHz F_{OUT} (±15 MHz) (700 MHz REFCLK)	Full	V		65		dBc
180 MHz F_{OUT} (±1 MHz) (700 MHz REFCLK)	Full	V		80		dBc
180 MHz F_{OUT} (±50 kHz) (700 MHz REFCLK)	Full	V		84		dBc
OUTPUT PHASE NOISE CHARACTERISTICS (@ 103 MHz I_{OUT})						
@ 1 kHz Offset	Full	V		–147		dBc/Hz
@ 10 kHz Offset	Full	V		–150		dBc/Hz
@ 100 kHz Offset	Full	V		–152		dBc/Hz
OUTPUT PHASE NOISE CHARACTERISTICS (@ 403 MHz I_{OUT})						
@ 1 kHz Offset	Full	V		–133		dBc/Hz
@ 10 kHz Offset	Full	V		–137		dBc/Hz
@ 100 kHz Offset	Full	V		–140		dBc/Hz

Parameter	Temp	Test Level	Min	Typ	Max	Unit
OUTPUT PHASE NOISE CHARACTERISTICS (@ 100 MHz I_{OUT} with 700 MHz REFCLK)						
@ 100 Hz Offset	Full	V	–125			dBc/Hz
@ 1 kHz Offset	Full	V	–140			dBc/Hz
@ 10 kHz Offset	Full	V	–148			dBc/Hz
@ 100 kHz Offset	Full	V	–150			dBc/Hz
@ 1 MHz Offset	Full	V	–150			dBc/Hz
@ 10 MHz Offset	Full	V	–150			dBc/Hz
PHASE DETECTOR AND CHARGE PUMP						
Phase Detector Frequency	Full	VI			150	MHz
Phase Detector Frequency (Divide-by-4 Enabled)[4]	Full	VI			400	MHz
Charge Pump Sink and Source Current[5]	Full	VI			4	mA
Fast Lock Current (Acquisition Only)	Full	VI			7	mA
Open-Loop Current (Acquisition Only)	Full	VI			30	mA
Sink and Source Current Absolute Accuracy[6]	Full	V		2.5		%
Sink and Source Current Matching[6]	Full	V		1		%
Input Sensitivity PD_{IN} and DIV_{IN} (50 Ω)[7]	Full	IV	–15		0	dBm
Input Impedence PD_{IN} and DIV_{IN} (Single-Ended)	Full	V		1		kΩ
Phase Noise @ 100 MHz Input Frequency						
@ 10 kHz Offset	Full	V		110		dBc/Hz
@ 100 kHz Offset	Full	V		140		dBc/Hz
@ 1 MHz Offset	Full	V		148		dBc/Hz
Charge Pump Output Range[8]	Full	V			CPV_{DD}	V
MIXER						
IF_{OUT}[9]	Full	V		400		MHz
F_{RF}	Full	VI			2	GHz
F_{LO}	Full	VI			2	GHz
Conversion Gain	Full	VI	0.0	3.5		dB
LO Level	Full	VI	–10		+5	dBm
RF Level	Full	VI	–20			dBm
Input IP3	Full	VI	5	9		dBm
1 dB Input Compression Power[10]	Full	VI	–3			dBm
Input Impedance (Single-Ended)						
LO	Full	V		1		kΩ
RF	Full	V		1		kΩ
LOGIC INPUTS						
Logic 1 Voltage	Full	VI	2.0			V
Logic 0 Voltage	Full	VI			0.8	V
Logic 1 Current	Full	VI			12	µA
Logic 0 Current	Full	VI			12	µA
Input Capacitance	Full	V		3		pF
POWER SUPPLY						
P_{DISS} (Worst-Case Conditions—Everything on P_{FD} Input Frequency 150 MHz)	Full	VI		2	2.5	W
P_{DISS} (DAC and DDS Core Only Worst-Case)	Full	VI		1.7	2	W
P_{DISS} (Power-Down Mode)	Full	VI		65	100	mW
P_{DISS} Mixer Only	Full	VI		60	75	mW
P_{DISS} PFD and CP (@ 100 MHz) Only	Full	VI		350	435	mW

Parameter	Temp	Test Level	Min	Typ	Max	Unit
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	Full	IV			10	MHz
Minimum Clock Pulse Width Low (t_{PWL})	Full	IV	5.5			ns
Minimum Clock Pulse Width High (t_{PWH})	Full	IV	15			ns
Maximum Clock Rise/Fall Time	Full	IV			1	ms
Minimum Data Setup Time (t_{DS})	Full	IV	7			ns
Mimimum Data Hold Time (t_{DH})	Full	IV	0			ns
Maximum Data Valid Time (t_{DV})	Full	IV			20	ns
Parallel Control Bus						
$\overline{WR}$ Minimum Low Time	Full	IV	3			ns
$\overline{WR}$ Minimum High Time	Full	IV	6			ns
$\overline{WR}$ Minimum Period	Full	IV	9			ns
Address to $\overline{WR}$ Setup (T_{ASU})	Full	IV	3			ns
Address to $\overline{WR}$ Setup (T_{AHU})	Full	IV	0			ns
Data to $\overline{WR}$ Setup (T_{DSU})	Full	IV	3.5			ns
Data to $\overline{WR}$ Hold (T_{DHU})	Full	IV	0			ns
Miscellaneous Timing Specifications						
REFCLK to SYNCLK	Full	V		2.5		ns
FUD to SYNCLK Setup Time	Full	IV	4			ns
FUD to SYNCLK Hold Time	Full	IV	0			ns
REFCLK to SYNCLK Delay	Full	IV		2.5	3	ns
FUD Rising Edge to Frequency Change						
Single Tone Mode	25°C	IV			83	sysclk cycles
Linear Sweep Mode	25°C	IV			99	sysclk cycles
FUD Rising Edge to Phase Offset Change	25°C	IV			83	sysclk cycles

[1] The reference clock input is configured to accept a differential or single-ended sine wave input or a 3 V CMOS-level pulse input.
[2] REFCLK input is internally dc biased. AC coupling should be used.
[3] Reference clock frequency is selected to ensure second harmonic is out of the bandwidth of interest.
[4] PD inputs sent @ 400 MHz, with divide-by-4 enabled.
[5] The charge pump current is programmable in eight discrete steps, minimum value assumes current sharing.
[6] For 0.75 V < V_{CP} < CPV_{DD} – 0.75 V.
[7] These differential inputs are internally dc biased. AC coupling should be used.
[8] The charge pump supply voltage can range from 4.75 V to 5.25 V.
[9] Output interface is differential open collector.
[10] For 1 dB output compression; input power measured at 50 Ω.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AV_{DD}	4 V
DV_{DD}	4 V
CPV_{DD}	6 V
Digital Input Voltage	–0.7 V to $+V_{DD}$
Digital Output Current	5 mA
Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
θ_{JA} EPAD Soldered	25°C/W

Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

Table 3. Explanation of Test Levels

I	100% Production Tested.
III	Sample Tested Only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

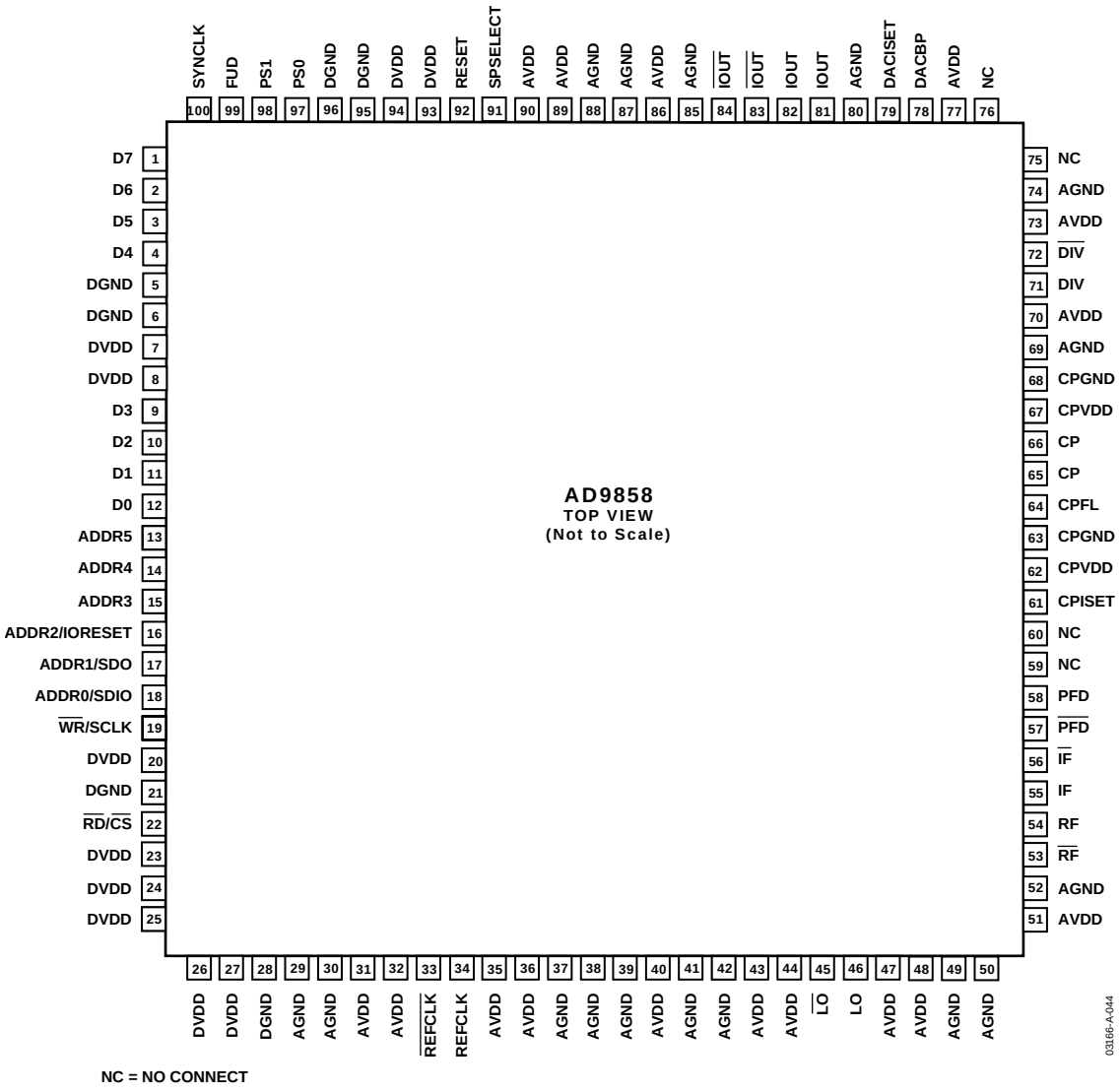


Figure 2. 100-Lead EPAD (SV-100) Pin Configuration

PIN FUNCTION DESCRIPTIONS

Table 4. Pin Function Descriptions—100-Lead EPAD (SV-100)

Pin No.	Mnemonic	I/O	Description
1 to 4, 9 to 12	D7 to D0	I	Parallel Port DATA. Note that the functionality of these pins is valid only when the I/O port is configured as a parallel port.
5, 6, 21, 28, 95, 96	DGND		Digitial Ground.
7, 8, 20, 23 to 27, 93, 94	DVDD		Digital Supply Voltage.
13 to 18	ADDR5 to ADDR0	I	When the I/O port is configured as a parallel port, these pins serve as a 6-bit address select for accessing the on-chip registers (see the IORESET, SDO, and SDIO pins below for serial port mode).
16	IORESET	I	Note that this is valid only for serial programming mode. Active high input signal that resets the serial I/O bus controller. It is intended to serve as a means of recovering from an unresponsive serial bus caused by improper programming protocol. Asserting an I/O reset does not affect the contents of previously programmed registers nor does it invoke their default values.
17	SDO	O	Note that this is valid only for serial programming mode. When operating the I/O port as a 3-wire serial port, this pin serves as a unidirectional serial data output pin. When operated as a 2-wire serial port, this pin is unused.
18	SDIO	I or I/O	Note that this is valid only for serial programming mode. When operating the I/O port as a 3-wire serial port, this pin is the serial data input. When operated as a 2-wire serial port, this pin is the bidirectional serial data pin.
19	$\overline{WR}$/SCLK	I	When the I/O port is configured for parallel programming mode, this pin functions as an active low write pulse ($\overline{WR}$). When configured for serial programming mode, this pin functions as the serial data clock (SCLK).
22	$\overline{RD}$/$\overline{CS}$	I	When the I/O port is configured for parallel programming mode, this pin functions as an active low read pulse ($\overline{RD}$). When configured for serial programming mode, this pin functions as an active low chip select ($\overline{CS}$) that allows multiple devices to share the serial bus.
29, 30, 37 to 39, 41, 42, 49, 50, 52, 69, 74, 80, 85, 87, 88	AGND	I	Analog Ground.
31, 32, 35, 36, 40, 43, 44, 47, 48, 51, 70, 73, 77, 86, 89, 90	AVDD	I	Analog Supply Voltage.
33	$\overline{REFCLK}$	I	Reference Clock Complementary Input. (Note that when the REFCLK port is operated in single-ended mode, $\overline{REFCLK}$ should be decoupled to AVDD with a 0.1 µF capacitor.
34	REFCLK	I	Reference Clock Input.
45	$\overline{LO}$	I	Mixer Local Oscillator (LO) Complementary Input. Note that when the LO port is operated in single-ended mode, $\overline{LO}$ should be decoupled to AVDD with a 0.1 µF capacitor.
46	LO	I	Mixer Local Oscillator (LO) Input.
53	$\overline{RF}$	I	Analog Mixer RF Complementary Input. Note that when the RF port is operated in single-ended mode, $\overline{RF}$ should be decoupled to AVDD with a 0.1 µF capacitor.
54	RF	I	Analog Mixer RF Input.
55	IF	O	Analog Mixer IF Output.
56	$\overline{IF}$	O	Analog Mixer IF Complementary Output.
57	$\overline{PFD}$	I	Phase Frequency Detector Complementary Input . Note that when the PFD port is operated in single-ended mode, $\overline{PFD}$ should be decoupled to AVDD with a 0.1 µF capacitor.
58	PFD	I	Phase Frequency Detector Input.
59, 60, 75, 76	NC		No Connection.
61	CPISET	I	Charge Pump Output Current Control. A resistor connected from CPISET to CPGND establishes the reference current for the charge pump.
62, 67	CPVDD	I	Charge Pump Supply Voltage.
63, 68	CPGND	I	Charge Pump Ground.
64	CPFL	O	Charge Pump Fast Lock Output.
65, 66	CP	O	Charge Pump Output.

Pin No.	Mnemonic	I/O	Description
71	DIV	I	Phase Frequency Detector Feedback Input.
72	$\overline{\text{DIV}}$	I	Phase Frequency Detector Feedback Complementary Input. Note that when the DIV port is operated in single-ended mode, $\overline{\text{DIV}}$ should be decoupled to AVDD with a 0.1 µF capacitor.
78	DACBP		DAC Baseline Decoupling Pin, Typically Bypassed to Pin 77 with a 0.1 µF Capacitor.
79	DACISET	I	A Resistor Connected from DACISET to AGND Establishes the Reference Current for the DAC.
81, 82	IOUT	O	DAC Output.
83, 84	$\overline{\text{IOUT}}$	O	DAC Complementary Output.
91	SPSELECT	I	I/O Port Serial/Parallel Programming Mode Select Pin. Logic 0: serial programming mode. Logic 1: parallel programming mode.
92	RESET	I	Active High Hardware Reset Pin. Assertion of the RESET pin forces the AD9858 to its default operating conditions.
97, 98	PS0, PS1	I	Used to Select One of the Four Internal Profiles. These pins are synchronous to the SYNCLK output.
99	FUD	I	Frequency Update. The rising edge transfers the contents of the internal buffer registers to the memory registers. This pin is synchronous to the SYNCLK output.
100	SYNCLK	O	Clock Output Pin that Serves as a Synchronizer for External Hardware. SYNCLK runs at REFCLK/8.

TYPICAL PERFORMANCE CHARACTERISTICS

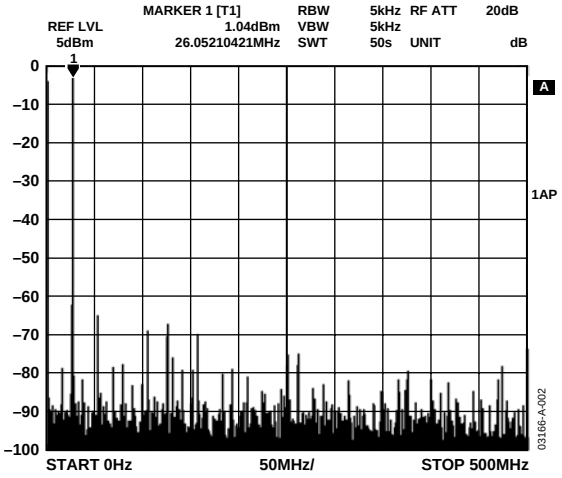


Figure 3. Wideband SFDR, 26 MHz F_{OUT}

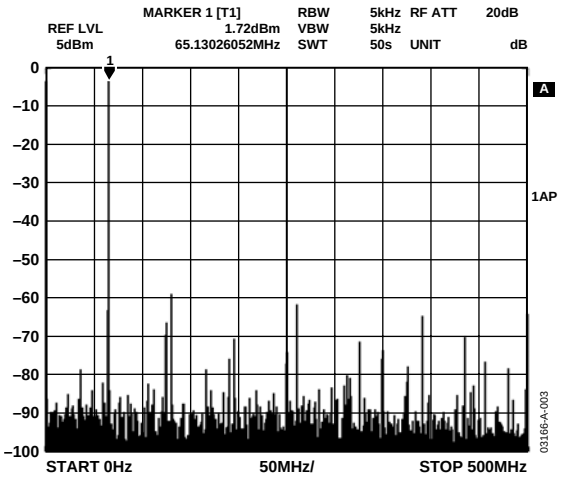


Figure 4. Wideband SFDR, 65 MHz F_{OUT}

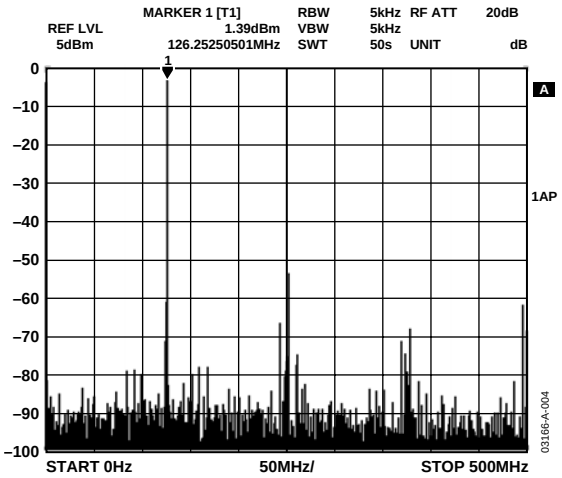


Figure 5. Wideband SFDR, 126 MHz F_{OUT}

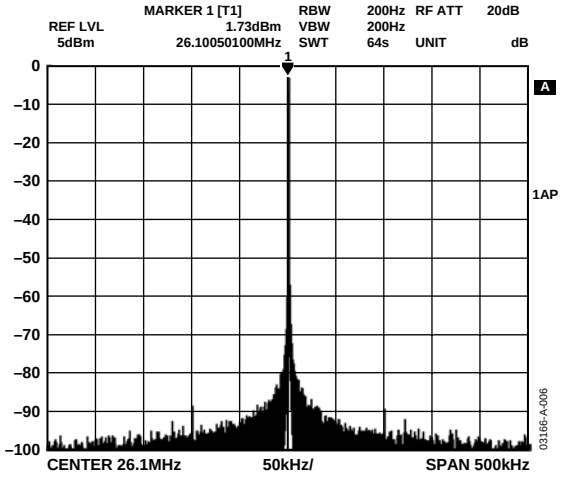


Figure 6. Narrow-Band SFDR, 26 MHz F_{OUT}, 1 MHz BW

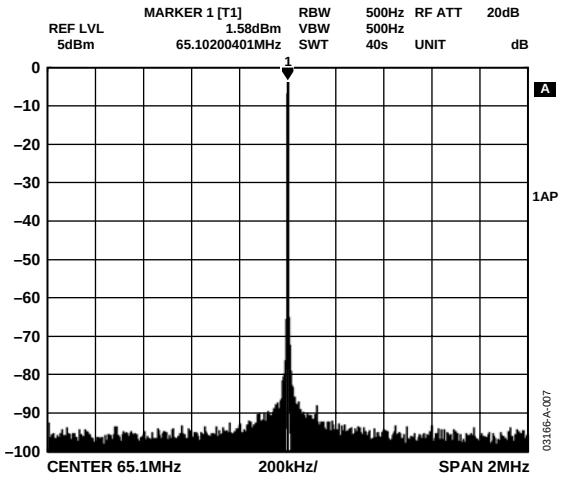


Figure 7. Narrow-Band SFDR, 65 MHz F_{OUT}, 1 MHz BW

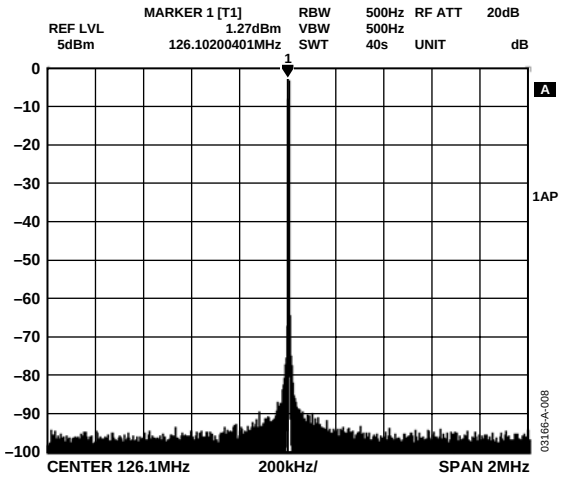


Figure 8. Narrow-Band SFDR, 126 MHz F_{OUT}, 1 MHz BW

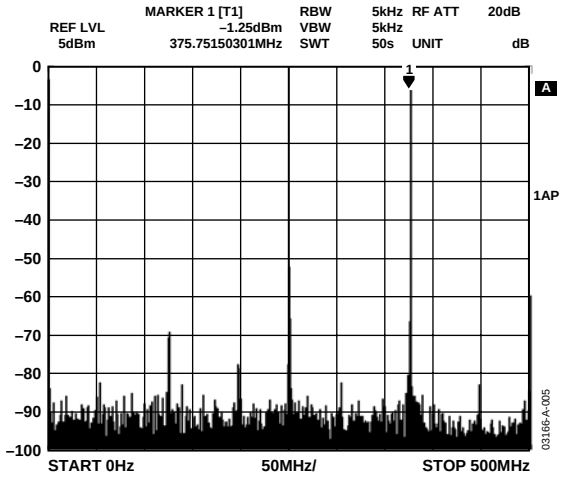


Figure 9. Wideband SFDR, 375 MHz F_{OUT}

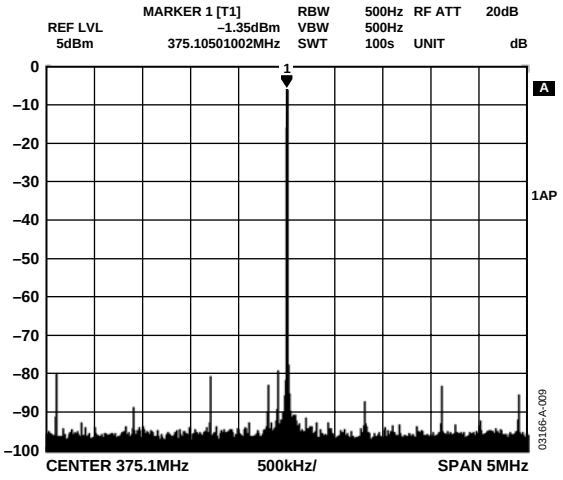


Figure 12. Narrow-Band SFDR, 375 MHz F_{OUT}, 1 MHz BW

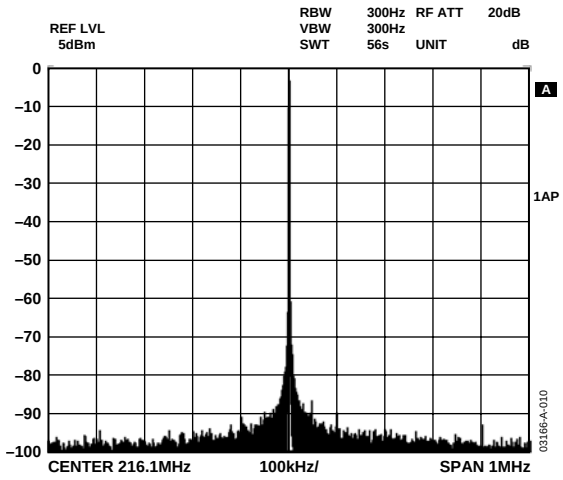


Figure 10. Narrow-Band SFDR, 201 MHz F_{OUT}, 1 MHz BW, 1 GHz Clock, Divider Off

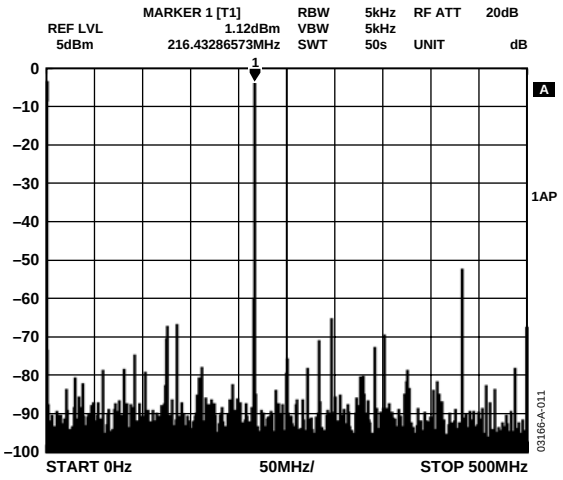


Figure 13. Wideband SFDR, 201 MHz F_{OUT}, 1GHz Clock, Divider Off

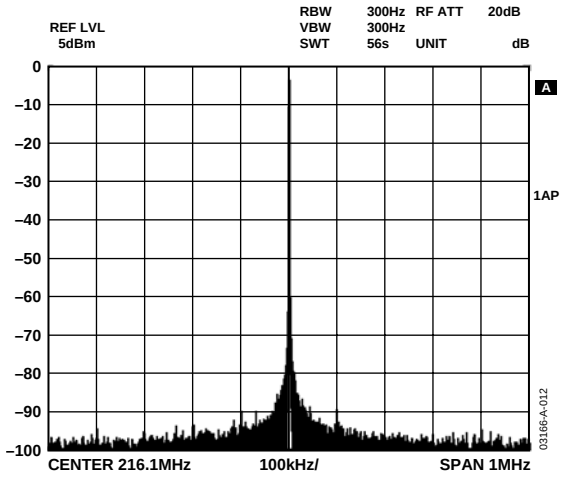


Figure 11. Narrow-Band SFDR, 201 MHz F_{OUT}, 1 MHz BW, 2 GHz Clock, Divider On

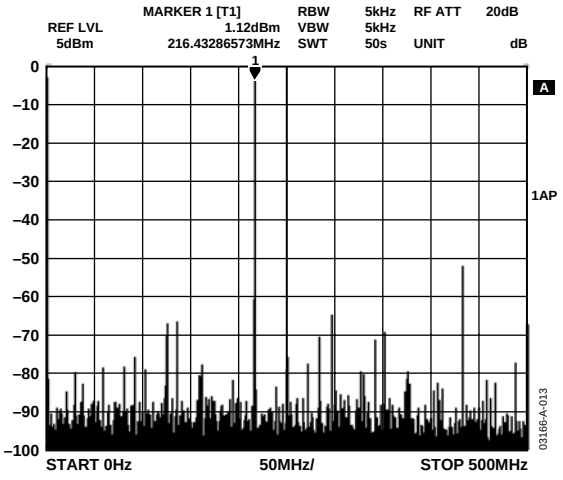


Figure 14. Wideband SFDR, 201 MHz F_{OUT}, 2 GHz Clock, Divider On

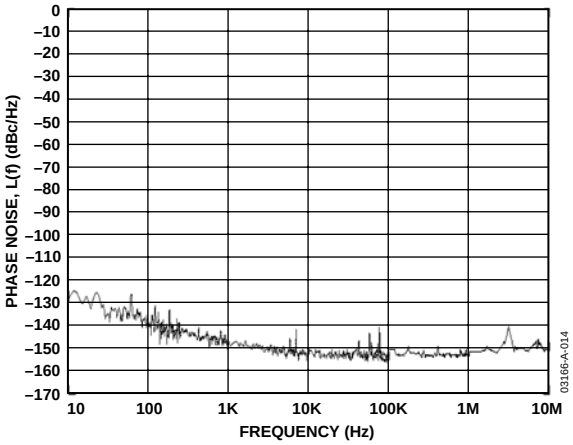


Figure 15. Residual Phase Noise, 103 MHz F_{OUT}, 1 GHz REFCLK

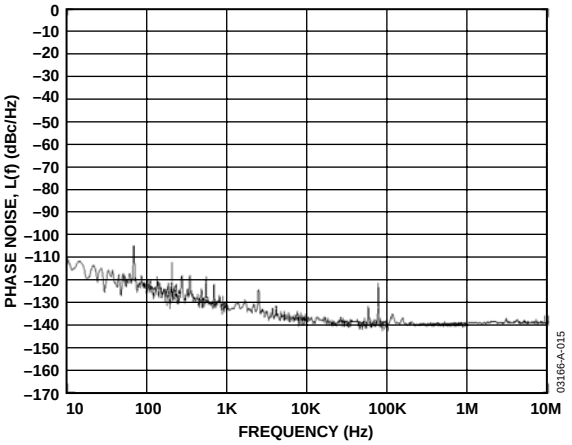


Figure 18. Residual Phase Noise, 403 MHz F_{OUT}, 1 GHz REFCLK

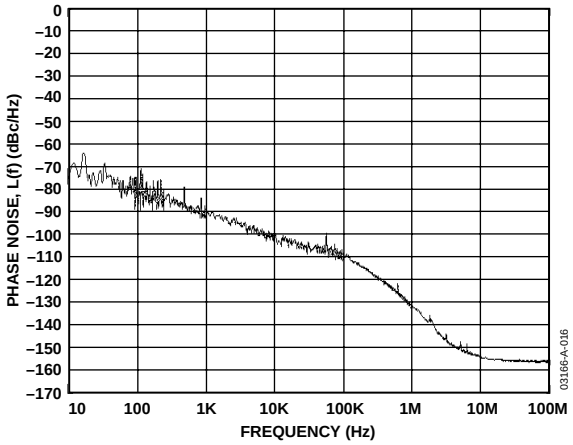


Figure 16. Fractional Divider Loop Residual Phase Noise, F_{IN} = 115 MHz, F_{OUT} = 1550 MHz, Loop BW = 50 kHz

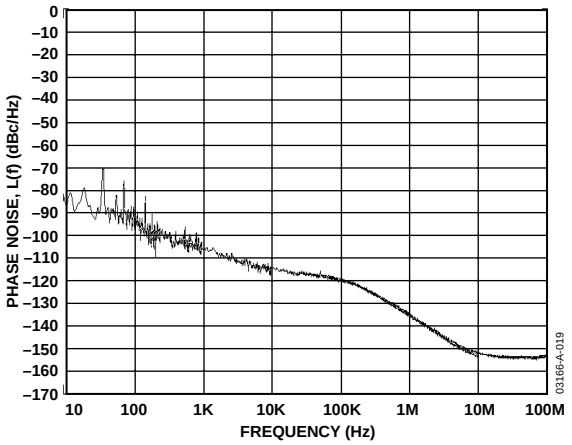


Figure 19. Translation Loop Residual Phase Noise F_{LO} = 1500 MHz, F_{OUT} = 1550 MHz, Loop BW = 50 kHz

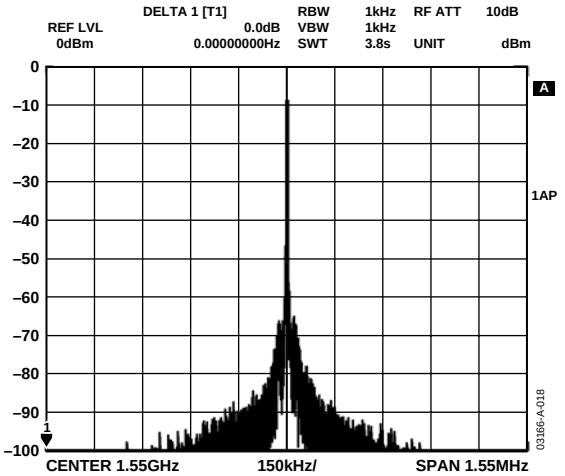


Figure 17. Fractional Divider Loop SFDR, F_{IN} = 96.9 MHz, F_{OUT} = 1550 MHz, BW = 1.5 MHz

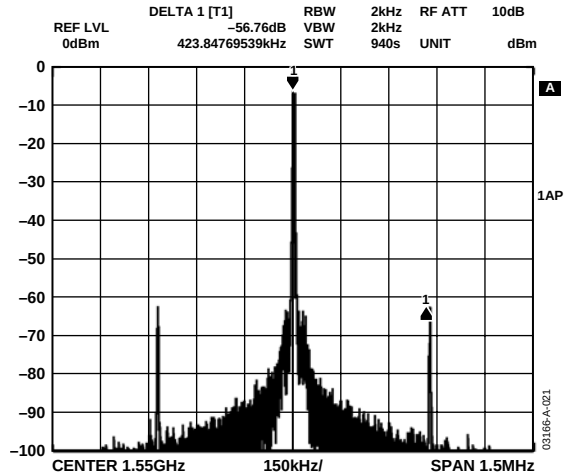


Figure 20. Fractional Divider Loop SFDR, F_{IN} = 97.3 MHz, F_{OUT} = 1550 MHz, BW = 1.5 MHz

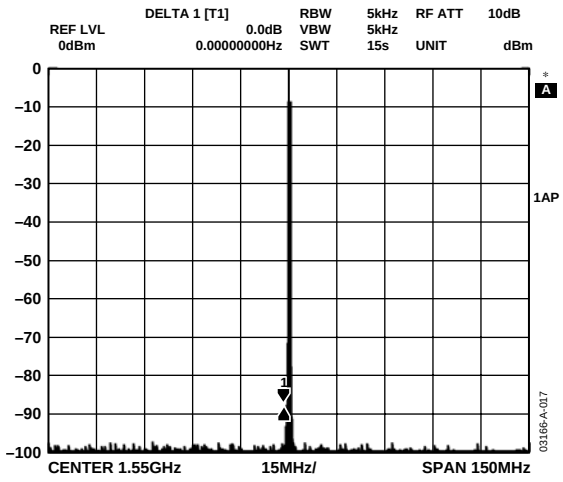


Figure 21. Fractional Divider Loop SFDR, F_{IN} = 96.9 MHz, F_{OUT} = 1550 MHz, BW = 150 MHz

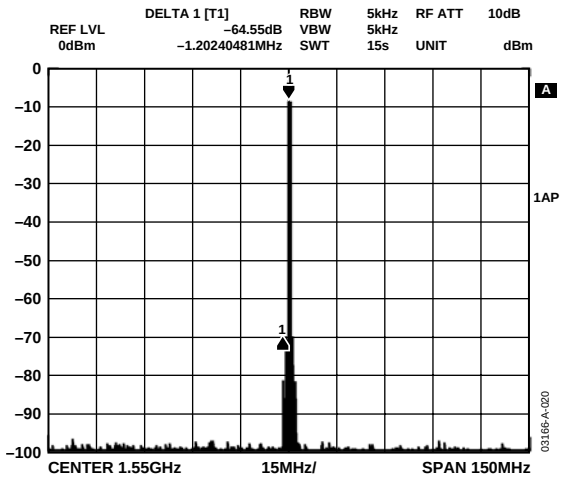


Figure 24. Fractional Divider Loop SFDR, F_{IN} = 97.3 MHz, F_{OUT} = 1550 MHz, BW = 150 MHz

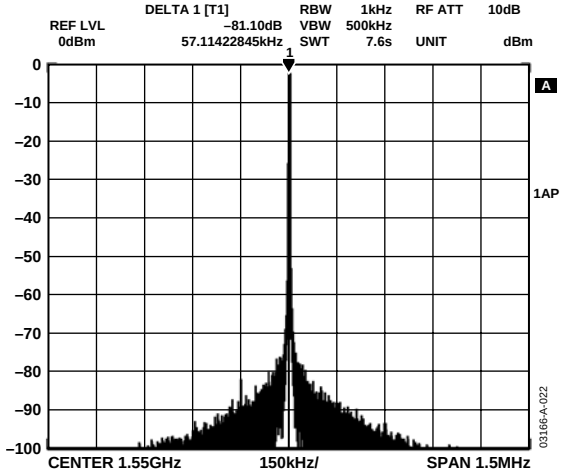


Figure 22. Translation Loop SFDR, F_{LO} = 1459 MHz, F_{OUT} = 1550 MHz, BW = 1.5 MHz

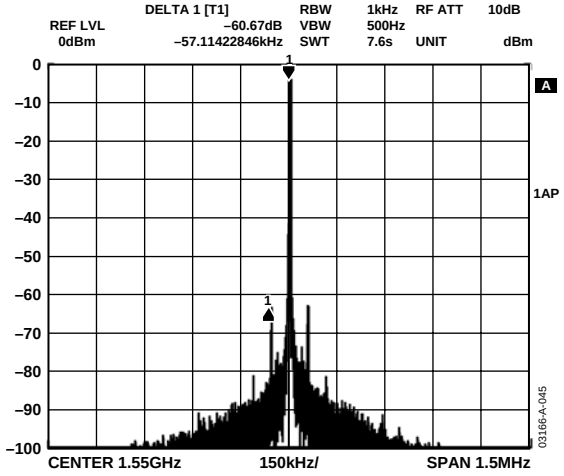


Figure 25. Translation Loop SFDR, F_{LO} = 1410 MHz, F_{OUT} = 1550 MHz, BW = 1.5 MHz

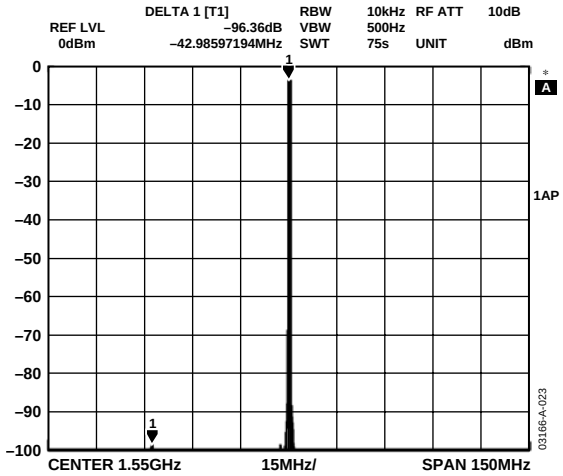


Figure 23. Translation Loop SFDR, F_{LO} = 1459 MHz, F_{OUT} = 1550 MHz, BW = 150 MHz

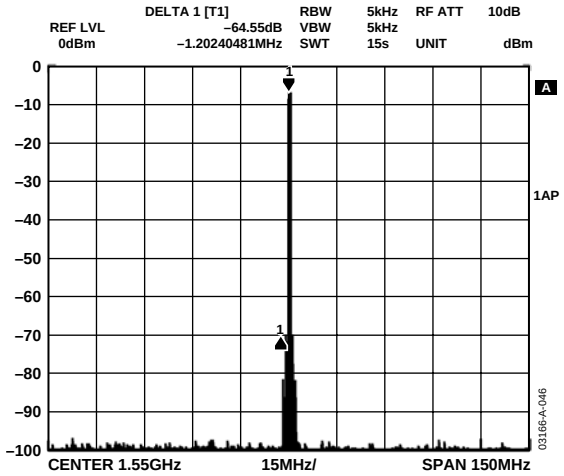


Figure 26. Translation Loop SFDR, F_{LO} = 1410 MHz, F_{OUT} = 1550 MHz, BW = 150 MHz

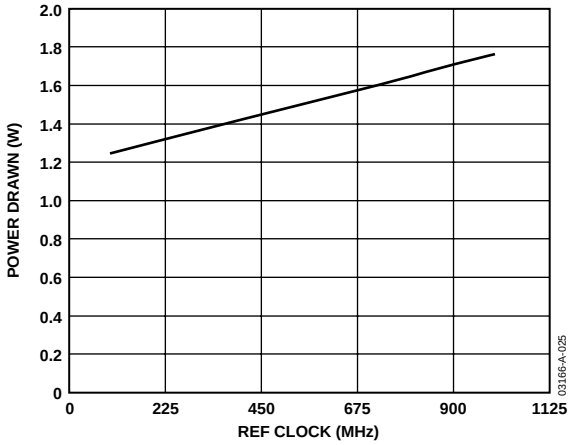


Figure 27. Supply Current vs. REFCLK (F_{OUT} = REFCLK/5)

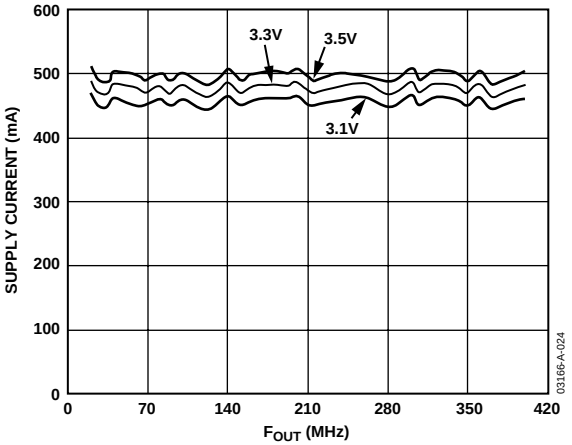


Figure 28. Supply Current vs. F_{OUT} (1 GHz REFCLK)

THEORY OF OPERATION

OVERVIEW

The AD9858 direct digital synthesizer (DDS) is a flexible device that can address a wide range of applications. The device consists of an NCO with a 32-bit phase accumulator, 14-bit phase offset adjustment, a power efficient DDS core, and a one giga-samples per second (1 GSPS) 10-bit digital-to-analog converter. The AD9858 incorporates additional capabilities for automated frequency sweeping. The device also offers an analog mixer capable of operating at 2 GHz, a phase-frequency detector (PFD), and a programmable charge pump (CP) with advanced fast-lock capability. These RF building blocks can be used for various frequency synthesis loops or as needed in system design.

The AD9858 can directly generate frequencies up to 400+ MHz when driven at a 1 GHz internal clock speed. This clock can be derived from an external clock source of up to 2 GHz by using the on-chip divide-by-2 feature. The on-chip mixer and PFD/CP make possible a variety of synthesizer configurations capable of generating frequencies in the 1 GHz to 2 GHz range or higher.

The AD9858 offers the advantages of a DDS with the additional flexibility to work in concert with analog frequency synthesis techniques (PLL, mixing) to generate precision frequency signals with high frequency resolution, fast frequency hopping, fast settling time, and automated frequency sweeping capabilities.

Writing data to its on-chip digital registers that control all operations of the device easily configures the AD9858. The AD9858 offers a choice of both serial and parallel ports for controlling the device. Four user profiles can be selected by a pair of external pins. These profiles allow independent setting of the frequency tuning word and the phase offset adjustment word for each of four selectable configurations.

The AD9858 can be programmed to operate in single-tone mode or in frequency-sweeping mode. To save on power consumption, there is also a programmable full-sleep mode, during which most of the device is powered down to reduce current flow.

The operation of a DDS is described in detail in a tutorial available from Analog Devices at www.analog.com/dds.

COMPONENT BLOCKS

DDS Core

The DDS core generates the numeric values that represent a sinusoid in the digital domain. Depending on the operating mode of the DDS, this sinusoid may be changed in frequency, phase, or perhaps modulated by an information carrying signal. The frequency of the output signal is determined by a user-programmed frequency tuning word (FTW). The relation of the output frequency of the device to the system clock (SYSCLK) is determined by the following equation:

$$F_O = \frac{(FTW \times SYSCLK)}{2^N}$$

where for the AD9858, $N = 32$.

For a more detailed explanation of a DDS core, consult the DDS tutorial at www.analog.com/dds.

DAC Output

The AD9858 incorporates an integrated 10-bit current output DAC. Two complementary outputs provide a combined full-scale output current (I_{OUT}). Differential outputs reduce the amount of common-mode noise that might be present at the DAC output, offering the advantage of an increased signal-to-noise ratio. The full-scale current is controlled by means of an external resistor (R_{SET}) connected between the DACISET pin and analog ground. The full-scale current is proportional to the resistor value as follows:

$$R_{SET} = 39.19 / I_{OUT}$$

The maximum full-scale output current of the combined DAC outputs is 40 mA, but limiting the output to 20 mA provides the best spurious-free dynamic range (SFDR) performance. The DAC output compliance range is (AV_{DD} – 1.5 V) to (AV_{DD} + 0.5 V). Voltages developed beyond this range cause excessive DAC distortion and could potentially damage the DAC output circuitry. Proper attention should be paid to the load termination to keep the output voltage within this compliance range. When terminating the differential outputs into a transformer, the center tap should be attached to AV_{DD}.

PLL Frequency Synthesizer

The PLL frequency synthesizer is a group of independent synthesis blocks, designed to be used with the DDS to expand the range of synthesis applications. These blocks are a digital phase-frequency detector (PFD) that drives a charge pump (CP). The charge pump incorporates fast-locking logic, described below. Based on system requirements, the user supplies an external loop filter and one or more VCOs. A high speed analog mixer is included for translation synthesis loops. Using the different blocks in the PLL frequency synthesizer in conjunction with the DDS, the user can create translation loops (also known as offset loops), fractional divider loops, as well as traditional PLL loops to multiply the output of the DDS in frequency.

Phase-Frequency Detector

The phase detector has two inputs, PD_{IN} and DIV_{IN}. Both are analog inputs that can be operated in differential or single-ended mode. Both are designed to operate at frequencies up to 150 MHz, although signals of up to 400 MHz can be accommodated on the inputs when the divide-by-4 functions are used. The expected input level for both the PD and DIV inputs is in the range of 800 mV p-p (differential), 400 mV p-p (single-ended). A programmable divider that offers division ratios of M, N = {1, 2, 4} immediately follows the input. The division ratio is controlled by means of the control function register.

Charge Pump

The charge pump output reference current is determined by an external resistor (~2.4 kΩ), which establishes a 500 µA maximum internal baseline current (I_{CP0}). The baseline current is scaled to provide the appropriate drive current for the CP's various operating modes (frequency detect mode, wide closed-loop, and final closed-loop). The amount of scaling in each mode is programmable by means of the values stored in the control function register, giving the user maximum flexibility of the PLL's frequency locking capability.

The CP polarity can be configured as either positive or negative with respect to the PD input. When the CP polarity is positive, if the DIV input leads the PD input, the charge pump attempts to decrease the voltage at the VCO control node. If the DIV input lags the PD input, the charge pump works to increase the voltage at the VCO control node. When the CP polarity is negative, the opposite occurs. This allows the user to define either input as the feedback path. This also allows the AD9858 to accommodate ground-referenced or supply-referenced VCOs. This functionality is defined by the charge pump polarity (CPP) bit in the control function register. When CPP = 0 (default), the charge pump is set up for operation with a ground-referenced VCO. When CPP = 1, the charge pump is set up for a supply-referenced VCO.

Internal to the CP, the I_{CP0} current is scaled to provide different output drive current values for the various modes of operation. In its normal operating mode, the final closed-loop mode can be programmed to scale I_{CP0} by 1, 2, 3, or 4. Setting the charge pump current offset bit, CFR<13>, applies a 2 mA offset to the programmed charge pump current, allowing scaler values of I_{CP0} of 5, 6, 7, or 8. The wide closed-loop mode can be programmed to scale I_{CP0} by 0, 2, 4, 6, 8, 10, 12, or 14. The frequency detect mode can be programmed to scale I_{CP0} by 0, 20, 40, or 60. The different modes of operation, controlled by the fast-locking logic, are discussed in the next section

The CP has an independent set of power pins that can operate at up to 5.25 V. While the device can operate from ground to rail, the voltage compliance should be kept in the range of 0.5 V to 4.5 V to ensure the best steady-state performance. The combination of programmable output current, programmable polarity, wide compliance range, and proprietary fast-lock capability offers the flexibility necessary for the digital PLL to operate within a broad range of PLL applications.

Fast-Locking Logic

The charge pump includes a fast-locking algorithm that helps to overcome the traditional limitations of PLLs with regard to frequency switching time. The fast-locking algorithm works in conjunction with the loop filter shown in Figure 29 to provide extremely fast frequency switching performance.

Based on the error seen between the feedback signal and the reference signal, the fast-locking algorithm puts the charge pump into one of three states: frequency detect mode, a wide closed-loop mode, and a final closed-loop mode. In the frequency detect mode, the feedback and reference signals are registering substantial phase and frequency errors. Rather than operating in a continuous closed-loop feedback mode, the charge pump supplies a fixed current of the correct polarity to the VCO control node that drives the loop towards frequency lock. Once frequency lock is detected, the fast-locking logic shifts the part into one of the closed-loop modes. In the closed-loop modes, either wide or final, the charge pump supplies current to the loop filter as directed by the phase-frequency detector PFD. The frequency-detect mode is intended to bring the system to a level of frequency lock from which the intermediary closed-loop system can quickly achieve phase lock.

The level of frequency lock accuracy aimed for is typically referred to as the lock range. Once the frequency is within the lock range, the time required to achieve phase lock can be determined by standard PLL transient analysis methods. Note that the charge pump current sources associated with the frequency detect mode are connected to Pin 64, while the closed loop current sources are connected to Pins 65 and 66. Pin 64 is connected directly to the loop filter zero compensation capacitor, as shown in Figure 29. This connection allows the smoothest transition from the frequency detect mode to the closed-loop modes and enables faster overall switching times. Pins 65 and 66 are connected to the loop filter in the conventional manner.

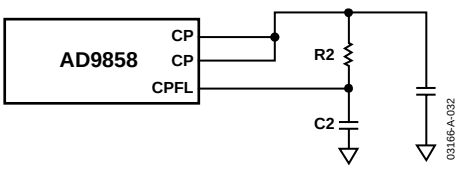


Figure 29. Symbolic Representation of Charge Pump to Loop Filter Connection

The frequency detection block works as follows. The comparison logic in the frequency detection circuitry operates one eighth of the DDS system clock. A comparison is made of the frequencies present at the PD input and the DIV input over 19 DDS clock cycles.

To ensure that frequency lock detection is achieved while the frequency difference is within the PLL lock range, the slew rate of the VCO input should be limited such that the lock range cannot be traversed within 152 system clock cycles. The slew rate of the VCO input is determined by the programmed level of frequency detect current and the size of the zero compensation capacitor according to the following relationship:

$$\frac{dv}{dt} = \frac{I_{f\,det}}{C_Z}$$

Once frequency detection occurs, the loop is closed and the loop is lock based on the current programmed for the wide closed-loop mode. It is important that the loop be designed for closed-loop stability while in the wide closed-loop mode. In this mode, less phase margin can usually be tolerated, because this mode is only used to enhance the lock time, but is not used in the "locked" free running state. Once the wide closed-loop mode achieves phase lock as determined by an internal lock detector, the phase-detector/charge pump transitions into the final closed-loop state. If no wide closed-loop current is programmed, the loop transitions directly from the frequency detect mode into the final closed-loop state. In the final closed-loop state, the loop characteristics should be optimized for the desired free running loop bandwidth.

The frequency detect mode is primarily useful in offset or translation loop applications where the phase detector inputs are more likely to detect large frequency transitions. For loop applications with significant amounts of division in the feedback loop, the frequency detection mode may not activate. This is due to the limited amount of frequency difference that is experienced at the phase detector inputs. For these applications, the primary means of accelerating the frequency settling time is to design the loop to acquire lock with the wide closed-loop setting and then switch to the final closed-loop setting.

As mentioned earlier, care should be taken when planning for a large transition using the frequency detect mode to ensure that the charge pump does not cause the VCO to overshoot the closed-loop lock range, as cycle slipping could occur, which would result in extended delays. Figure 30 shows two system responses. In the first, the charge pump output current is maximized during the frequency-detect mode so that, after 152 clock cycles, the VCO voltage has exceeded the closed-loop lock range. The second system provides less current during the frequency detect mode. While this results in a longer delay in approaching the closed-loop lock range, because the system does not exceed the closed-loop range, the fast-locking logic shifts the charge pump into intermediary closed-loop mode, resulting in a shorter overall frequency switching time.

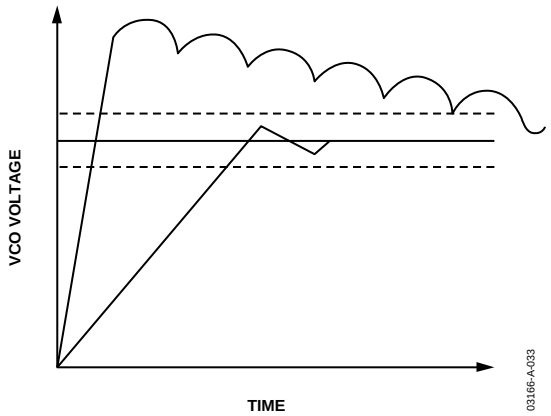


Figure 30. Symbolic Representation of Charge Pump to Loop Filter Connection

Analog Mixer

The analog mixer is included for translation loops, also known as offset loops. The radio frequency (RF) and local oscillator (LO) inputs are designed to operate at frequencies up to 2 GHz. Both inputs are differential analog input stages. Both input stages are internally dc biased and should be connected through an external ac coupling mechanism. The expected input level is in the range of 800 mV p-p (differential). The IF (intermediate frequency) output is a differential analog output stage designed to operate at frequencies less than 400 MHz. This mixer is based on the Gilbert cell architecture.

MODES OF OPERATION

The AD9858 DDS section has three modes of operation—single tone, frequency sweeping, and full sleep. The RF building blocks (PFD, CP, and mixer) can be active or powered down, used or unused, in either of the active modes.

In the single-tone mode, the device generates a single output frequency determined by a 32-bit word (frequency tuning word—FTW) loaded to an internal register. This frequency can be changed as desired, and frequency hopping can be accomplished at a rate limited only by the time required to update the appropriate registers. If even faster hopping is needed, the four profiles allow rapid hopping among the four frequencies stored in them by means of external select pins.

The frequency-sweeping mode allows for the automation of most of the frequency-sweeping task, making chirp and other frequency-sweeping applications possible without the inconvenience and possible speed limitations imposed by multiple register operations via the I/O port.

In whichever mode the device is operating, changes in frequency are phase continuous, which means that they do not cause discontinuities in the phase of the output signal. The first phase value after a frequency change is an increment of the last

phase value before the change, but at the new tuning word's phase increment value (FTW). (Note that this is not the same as phase-coherent over frequency changes; see Figure 31.)

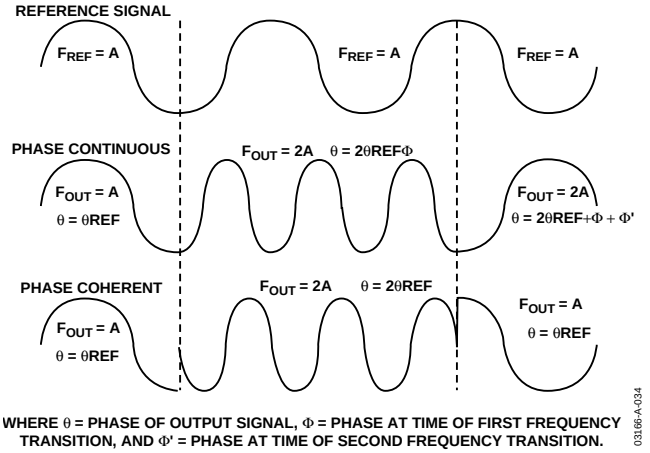


Figure 31. The Difference between a Phase Continuous Frequency Change and a Phase Coherent Frequency Change

Single-Tone Mode

When in single-tone mode, the AD9858 generates a signal, or tone, of a single desired frequency. This frequency is set by the value loaded by the user into the chip's frequency tuning word (FTW) register. This frequency can be between 0 Hz and somewhat below one-half of the DAC sampling frequency (SYSCLK). One-half of the sampling frequency is commonly called the Nyquist frequency. The practical upper limit to the fundamental frequency range of a DDS is determined by the characteristics of the external low-pass filter, known as the reconstruction filter, which must follow the DAC output of the DDS. This filter reconstructs the desired analog sine wave output signal from the stream of sampled amplitude values output by the DAC at the sample rate (SYSCLK).

A DDS is a sampled-data system. As the fundamental frequency of the DDS approaches the Nyquist frequency, the lower first image approaches the Nyquist frequency from above. As the fundamental frequency approaches the Nyquist frequency, it becomes difficult, and finally impossible, to design and construct a low-pass filter that will provide adequate attenuation for the first image frequency component.

The maximum usable frequency in the fundamental range of the DDS is typically between 40% and 45% of the Nyquist frequency, depending on the reconstruction filter. With a 1 GHz SYSCLK, the AD9858 is capable of producing maximum output frequencies of between 400 MHz and 450 MHz, depending on the reconstruction filter and the application system requirements.

For a desired output frequency (FO) and sampling rate (SYSCLK), the frequency tuning word (FTW) of the AD9858 is calculated according to the following equation

$$FTW = \left(FO \times 2^N\right) / SYSCLK$$

where N is the phase accumulator resolution in bits (32 in the AD9858), FO is in Hz, and the FTW is a decimal number.

Once a decimal number has been calculated, it must be rounded to an integer and converted to a 32-bit binary value. The frequency resolution of the AD9858 is 0.233 Hz when the SYSCLK is 1 GHz.

Frequency-Sweeping Mode

The AD9858 provides automated frequency sweeping capability. This allows the AD9858 to generate frequency-swept signals for chirped radar or other applications. The AD9858 includes features that automate much of the task of executing frequency sweeps.

The frequency sweep feature is implemented through the use of a frequency accumulator (not to be confused with the phase accumulator). The frequency accumulator repeatedly adds a frequency incremental quantity to the current value, thereby creating new instantaneous frequency tuning words, causing the frequency generated by the DDS to change with time. The frequency increment, or step size, is loaded into a register known as the delta frequency tuning word (DFTW). The rate at which the frequency is incremented is set by another register, the delta frequency ramp rate word (DFRRW). Together these two registers enable the AD9858 to sweep from a beginning frequency set by the FTW, upwards or downwards, at a desired rate and frequency step size. The result is a linear frequency sweep or chirp.

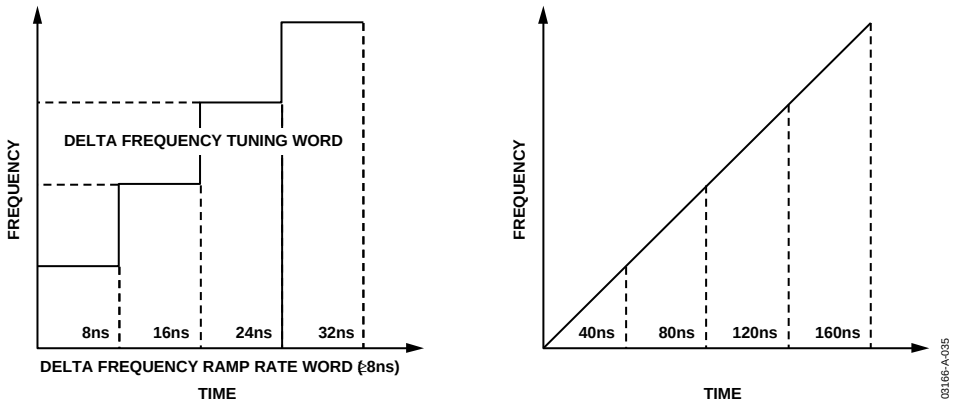


Figure 32. Frequency vs. Time Plots for a Given Sweep Profile

The delta frequency ramp rate word (DFRRW) functions as a countdown timer, in which the value of the DFRRW is decremented at the rate of SYSCLK/8. This means that the most rapid frequency word update occurs when a value of 1 is loaded into the DFRRW, and results in a frequency increment at 1/8 of the SYSCLK rate. With a SYSCLK of 1 GHz, the frequency can be incremented at a maximum rate of 125 MHz (DFRRW = 1). The delta frequency tuning word (DFTW) must specify whether the frequency sweep should proceed up or down from the starting frequency (FTW). Therefore, the DFTW is expressed as a twos complement binary value, in which positive indicates up and negative indicates down.

A DFRRW value of 0 written to the register stops all frequency sweeping. There is no automatic stop-at-a-given-frequency function. The user must calculate the time interval required to reach the final frequency and then issue a command to write 0 into the DFRRW register. The time required for a frequency sweep is calculated by the following formula

$$T = \frac{|f_F - f_S| \times 2^{34}}{SYSCLK^2} \times \frac{DFRRW}{DFTW}$$

where:

T is the duration of the sweep in seconds.

f_S is the starting frequency determined by

$$f_S = \frac{FTW}{2^{32}} \times SYSCLK \ .$$

f_F is the final frequency.

The delta frequency step size is given by

$$\Delta f = \frac{DFTW \times SYSCLK}{2^{31}} \ ,$$

remembering that DFTW is a signed (twos complement) value.

The time between each frequency step (Δt) is given by

$$\Delta t = \frac{8 \times DFRRW}{SYSCLK}$$

The value of the stop frequency f_F is determined by

$$f_F = f_S + T \times \frac{\Delta f}{\Delta t}$$

Returning to Starting Frequency

The original frequency tuning word (FTW), which was written into the frequency tuning register, does not change at any time during a sweeping operation. This means that the DDS may be returned to the sweep starting frequency at any time during a sweep. Setting the control bit named autoclear frequency accumulator forces the frequency accumulator to zero, instantly returning the DDS to the frequency stored as FTW.

Full-Sleep Mode

Setting all of the power-down bits in the control function register activates full-sleep mode. During the power-down condition, the clocks associated with the various functional blocks of the device are turned off, thereby offering a significant power savings.

SYNCHRONIZATION

SYNCLK and FUD Pins

Timing for the AD9858 is provided via the user-supplied REFCLK input. The REFCLK input is buffered and is the source for the internally generated SYSCLK. The frequency of SYSCLK can be either the same as REFCLK or half that of REFCLK (via a programmable divide-by-2 function set in the control function register CFR). The REFCLK input is capable of handling input frequencies as high as 2 GHz. However, the device is designed for a maximum SYSCLK frequency of 1 GHz. Thus, it is mandatory that the divide-by-2 SYSCLK function be enabled when the frequency of REFCLK is greater than 1 GHz.

SYSCLK serves as the sample clock for the DAC and is fed to a divide-by-8 frequency divider to produce SYNCLK. SYNCLK is provided to the user on the SYNCLK pin. This enables synchronization of external hardware with the AD9858's internal DDS clock. External hardware that is synchronized to the SYNCLK signal can then be used to provide the frequency update (FUD) signal to the AD9858. The FUD signal and SYNCLK are used to transfer the internal buffer register contents into the memory registers of the device. Figure 33 shows a block diagram of the synchronization methodology, and Figure 34 shows an I/O synchronization timing diagram.

Note that SYNCLK is also used to synchronize the assertion of the profile select pins (PS0, PS1). The FUD, PS0, and PS1 pins must be set up and held around the rising edge of SYNCLK. These device inputs are designed for zero hold time and 3.5 ns setup time.

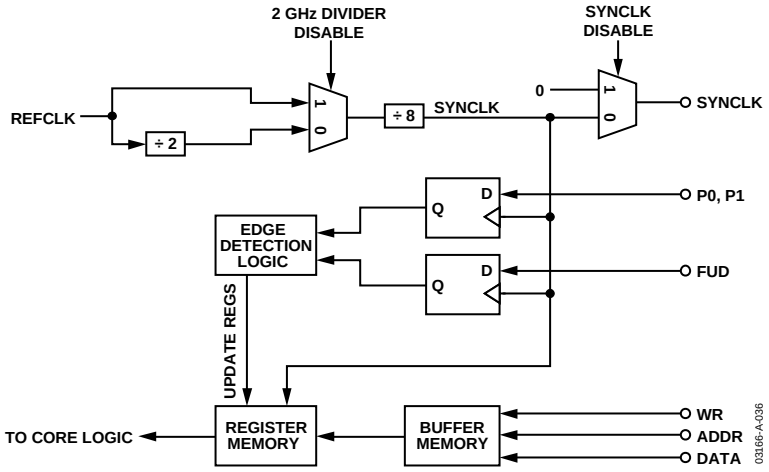


Figure 33. I/O Synchronization Block Diagram

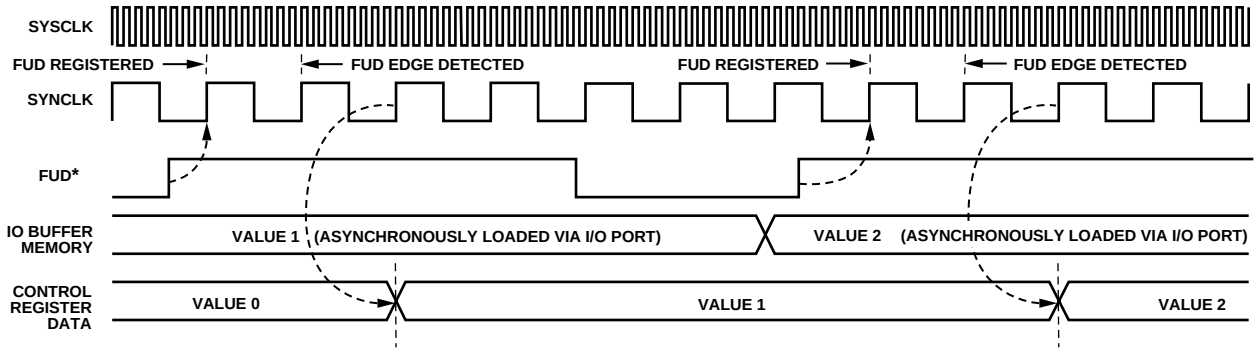


Figure 34. I/O Synchronization Timing Diagram

Frequency Planning

To achieve the best possible spurious performance when using the AD9858 in a hybrid synthesizer configuration, frequency planning can be employed. Frequency planning consists of being aware of the mechanisms that determine the location of the worst-case spurs and then using the appropriate loop tuning parameters to place these spurs either outside the loop bandwidth, such that they are attenuated, or completely outside the frequency range of interest.

When using the fractional divider configuration, the worst-case spurs occur whenever the images of the DAC harmonics fold back such that they are close to the DAC fundamental or carrier frequency. If these images fall within the loop bandwidth, they will be gained up by approximately 20 × log *N*, where *N* is the gain in the loop. If *N* is relatively high, these spurs can still realize significant gain even if they are slightly outside the loop bandwidth, since the loop attenuation rate is typically 20 dB/decade in this region. DAC images occur at

$$N \times F_{CLOCK} \pm M \times F_{OUT}$$

where *N* and *M* are integer multiples of F_{CLOCK} and F_{OUT}, respectively.

Figure 20 shows a high spurious condition where the low-order odd harmonics are folding back around the fundamental. Figure 21 shows that the worst spurs are confined to a narrow region around the carrier and that wideband spurs are attenuated. Figure 17 shows an alternate frequency plan that results in the same carrier frequency. Recall that the output frequency of the DAC is set by the equation

$$(F_{OUT} = F_{CLOCK} \times FTW/2^N)$$

This makes it possible to produce the same F_{OUT} by different combinations of F_{CLOCK} and *FTW*. In this case, the worst DAC spurs are placed well outside the loop bandwidth such that they are attenuated below the noise floor. Figure 24 shows a wideband plot for this frequency plan.

Other frequency combinations that can result in high spurious signals are when subharmonics of F_{CLOCK} fall within or near the loop bandwidth. To avoid this, ensure that the DAC F_{OUT} is sufficiently offset from the subharmonics of F_{CLOCK} such that these products are attenuated by the loop.

Frequency planning for the translation loop is similar in that the DAC images and the F_{CLOCK} subharmonics need to be considered. Figure 25 and Figure 26 show results for a high spurious configuration where odd order images are folding back close to the carrier. Figure 22 and Figure 23 show an alternative frequency plan that generates the same carrier frequency with low spurious content. Because this loop also requires a mixer LO frequency, additional care is required in planning for this frequency arrangement. Generally there is some mixer LO feedthrough. The amount of feedthrough depends on the PCB board layout isolation as well as the mixer LO power level, but levels of –80 dBc can typically be achieved. Figure 26 shows results for a situation where the mixer LO component shows up in the spectrum at 1.41 GHz, and another spur component shows up at *Mixer LO* + F_{CLOCK}/8. This places the mixer LO frequency well outside the bandwidth of interest, resulting in the spectrum shown in Figure 25.

PROGRAMMING THE AD9858

The transfer of data from the user to the DDS core of the device is a 2-step process. In a write operation, the user first writes the data to the I/O buffer using either the parallel port (which includes bits for address and data) or serial mode (where the address and data are combined in a serial word). Regardless of the method used to enter data to the I/O buffer, the DDS core cannot access the data until the data is latched into the memory registers from the I/O buffer. Toggling the FUD pin or changing one of the profile select pins causes an update of all elements of the I/O buffer memory into the DDS core's register memory.

I/O Port Functionality

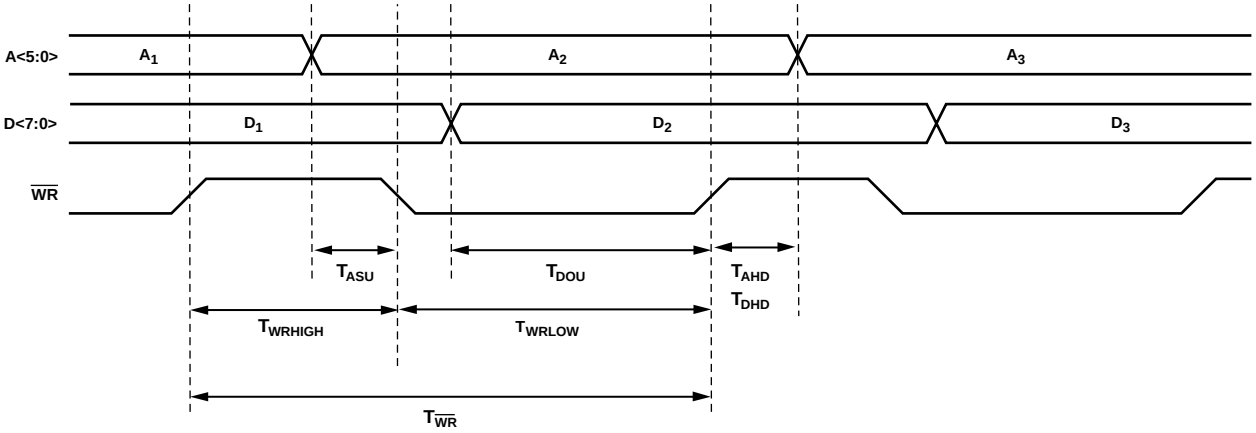
The I/O port can be operated in either serial or parallel programming mode. Mode selection is accomplished via the S/P Select pin. Logic 0 on this pin configures the I/O port for serial programming, while Logic 1 configures the I/O port for parallel programming.

The ability to read back the contents of a register is provided in both modes to facilitate the debug process during the user's prototyping phase of a design. In either mode, however, the reading back of profile registers requires that the profile select pins (P0, P1) be configured to select the desired register bank. When reading a register that resides in one of the profiles, the register address acts as an offset to select one of the registers among the group of registers defined by the profile. The profile select pins control the base address of the register bank and select the appropriate register grouping.

Parallel Programming Mode

In parallel programming mode, the I/O port makes use of eight bidirectional data pins (D7 to D0), six address input pins (ADDR5 to ADDR0), a read input pin ($\overline{RD}$), and a write input pin ($\overline{WR}$). A register is selected by providing the proper address combination as defined in the register map. Read or write functionality is invoked by pulsing the appropriate pin ($\overline{RD}$ or $\overline{WR}$); the two operations are mutually exclusive. The read or write data is transported on the D7 to D0 pins. The correlation between the D7 to D0 data bits and their functionality at a specific register address is detailed in the register map and register bit description.

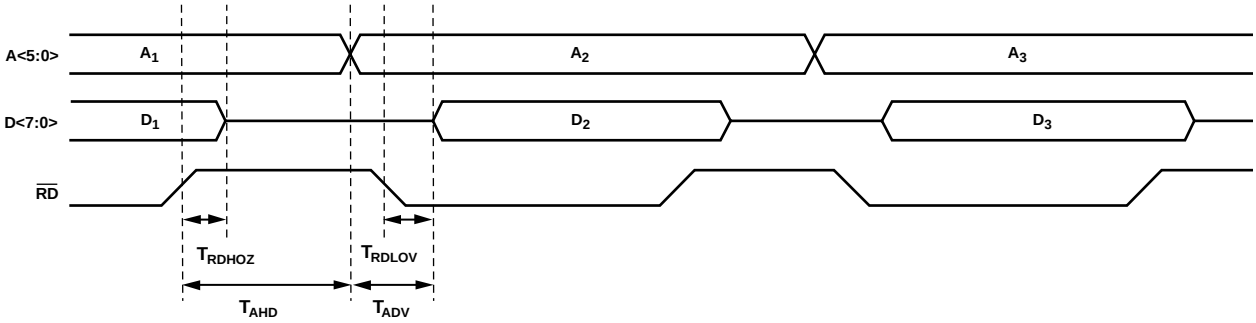
Parallel I/O operation allows write access to each byte of any register in the I/O buffer memory in a single I/O operation at a 100 MHz rate. However, unlike write operation, readback capability is *not* guaranteed at the 100 MHz rate. It is intended as a low speed function for debug purposes. Timing for both write and read cycles is depicted in Figure 35 and Figure 36.



SPECIFICATION	VALUE	DESCRIPTION
T_{ASU}	3ns	ADDRESS SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE
T_{DOU}	3.5ns	DATA SETUP TIME TO $\overline{WR}$ SIGNAL INACTIVE
T_{ADH}	0ns	ADDRESS HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
T_{DHD}	0ns	DATA HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
T_{WRLOW}	3ns	$\overline{WR}$ SIGNAL MINIMUM LOW TIME
T_{WRHIGH}	6ns	$\overline{WR}$ SIGNAL MINIMUM HIGH TIME
$T_{\overline{WR}}$	9ns	$\overline{WR}$ SIGNAL MINIMUM PERIOD

03166-A-038

Figure 35. I/O Port Write Cycle Timing (Parallel)



SPECIFICATION	VALUE	DESCRIPTION
T_{ASU}	15ns	ADDRESS TO DATA VALID TIME (MAXIMUM)
T_{ADH}	5ns	ADDRESS HOLD TIME TO $\overline{RD}$ SIGNAL INACTIVE (MINIMUM)
T_{RDLOV}	15ns	$\overline{RD}$ LOW TO OUTPUT VALID (MAXIMUM)
T_{RDHOZ}	10ns	$\overline{RD}$ HIGH TO DATA THREE-STATE (MAXIMUM)

03166-A-039

Figure 36. I/O Port Read Cycle Timing (Parallel)

Serial Programming Mode

In serial programming mode, the I/O port uses a chip select pin ($\overline{CS}$), a serial clock pin (SCLK), an I/O reset pin (IORESET), and either 1 or 2 serial data pins (SDIO and/or SDO). The number of serial data pins used depends on the configuration of the I/O port; i.e., whether it has been configured for 2-wire or 3-wire serial operation as defined by the control function register. In 2-wire mode, the SDIO pin operates as a bidirectional serial data pin. In 3-wire mode, the SDIO pin operates only as a serial data input pin, and the SDO pin acts as the serial output. The maximum rate of SCLK is 10 MHz; however, during read operation, the 10 MHz rate is not guaranteed.

The serial port is an SPI compatible serial interface and its operation is virtually identical to that of the AD9852/AD9854. Serial port communication occurs in two phases. Phase 1 is an instruction cycle consisting of an 8-bit word. The MSB of the instruction byte flags the ensuing operation as a read or write operation. The 6 LSBs define the serial address of the target register as defined in the register map. The instruction byte format is given in Table 5.

Table 5.

D7 (MSB)	D6	D5	D4	D3	D2	D1	DO (LSB)
1: Read 0: Write	X	A5	A4	A3	A2	A1	A0

Phase 2 of a serial port communication contains the data to be routed to/from the addressed register. The number of bytes transferred during Phase 2 depends on the length of the target register. Serial operation requires that *all* bits associated with a serial register address be transferred.

Both phases of a serial port communication require the serial data clock (SCLK) to be operating. When writing to the device, serial bits are transferred on the rising edge of SCLK. When reading from the device, serial output bits are transferred on the falling edge of SCLK. The bit order for both phases of a serial port communication is selectable via the control function register.

The $\overline{CS}$ pin serves as a chip select control line. When $\overline{CS}$ is at a Logic 1 state, the SDO and SDIO pins are disabled (forced into a high impedance state). Only when the $\overline{CS}$ pin is at a Logic 0 state are the SDO and SDIO pins active. This allows multiple devices to exist on a single serial bus. If multiple devices are connected to the same serial bus, then communication with a single device is accomplished by setting $\overline{CS}$ to a Logic 0 state on the target device, but to a Logic 1 state on all other devices. In this way, serial communication occurs only between the controller and the target device.

In the case where I/O synchronization is lost between the AD9858 and the external controller, the IORESET pin provides a means to re-establish synchronization without initializing the entire device. Asserting the active high IORESET pin resets the serial port state machine. This terminates the current I/O operation and puts the device into a state in which the next eight SCLK pulses are expected to be the instruction byte of the next I/O transfer. Note that any information previously written to the memory registers during the last valid communication cycle prior to loss of synchronization remains intact.

Register Map

The registers are listed in Table 6. The serial address and parallel address numbers associated with each of the registers are shown in hexadecimal format. Angle brackets <> are used to reference specific bits or ranges of bits. For example, <3> designates Bit 3, while <7:3> designates the range of bits from 7 down to 3, inclusive.

Table 6. Register Map

Register Name	Address Ser	Address Par	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value	Profile
Control Function Register (CFR)	0x00	0x00 <7:0>	Not Used	2 GHz Divider Disable	SYNCLK Out Disable	Mixer Power Down	Phase Detect PwrDwn	Power Down	SDIO Input Only	LSB First	0x18	N/A
		0x01 <15:8>	Freq. Sweep Enable	Enable Sine Output	Charge Pump Offset Bit	Phase Detector Divider Ratio (N) (see Table 10)		Charge Pump Polarity	Phase Detector Divider Ratio (M) (see Table 11)		0x00	N/A
		0x02 <23:16>	AutoClr Freq. Accum	AutoClr Phase Accum	Load Delta-Freq Timer	Clear Freq Accum	Clear Phase Accum	Open	Fast-Lock Enable	Don't Use FTW for Fast-Lock	0x00	N/A
		0x03 <31:24>	Frequency Detect Charge Pump Current (see Table 7)		Final Closed-Loop Charge Pump Current (see Table 8)			Wide Closed-Loop Charge Pump Current (see Table 9)			0x00	N/A
Delta-Freq Tuning Word (DFTW)	0x01	0x04	Delta Frequency Word <7:0>								–	N/A
		0x05	Delta Frequency Word <15:8>								–	N/A
		0x06	Delta Frequency Word <23:16>								–	N/A
		0x07	Delta Frequency Word <31:24>								–	N/A
Delta-Freq Ramp Rate (DFRRW)	0x02	0x08	Delta Frequency Ramp Rate Word <7:0>								–	N/A
		0x09	Delta Frequency Ramp Rate Word <15:8>								–	N/A
Frequency Tuning Word No. 0 (FTW0)	0x03	0x0A	Frequency Tuning Word No. 0 <7:0>								0x00	0
		0x0B	Frequency Tuning Word No. 0 <15:8>								0x00	0
		0x0C	Frequency Tuning Word No. 0 <23:16>								0x00	0
		0x0D	Frequency Tuning Word No. 0 <31:24>								0x00	0
Phase Offset Word 0 (POW0)	0x04	0x0E	Phase Offset Word No. 0 <7:0>								0x00	0
		0x0F	Not Used	Not Used	Phase Offset Word No. 0 <13:8>						0x00	0
Frequency Tuning Word No.1(FTW1)	0x05	0x10	Frequency Tuning Word No. 1 <7:0>								–	1
		0x11	Frequency Tuning Word No. 1 <15:8>								–	1
		0x12	Frequency Tuning Word No. 1 <23:16>								–	1
		0x13	Frequency Tuning Word No. 1 <31:24>								–	1
Phase Offset Word 1 (POW1)	0x06	0x14	Phase Offset Word No. 1 <7:0>								–	1
		0x15	Not Used	Not Used	Phase Offset Word No. 1 <13:8>						–	1
Frequency Tuning Word No. 2 (FTW2)	0x07	0x16	Frequency Tuning Word No. 2 <7:0>								–	2
		0x17	Frequency Tuning Word No. 2 <15:8>								–	2
		0x18	Frequency Tuning Word No. 2 <23:16>								–	2
		0x19	Frequency Tuning Word No. 2 <31:24>								–	2
Phase Offset Word 2 (POW2)	0x08	0x1A	Phase Offset Word No. 2 <7:0>								–	2
		0x1B	Not Used	Not Used	Phase Offset Word No. 2 <13:8>						–	2
Frequency Tuning Word No. 3 (FTW3)	0x09	0x1C	Frequency Tuning Word No. 3 <7:0>								–	3
		0x1D	Frequency Tuning Word No. 3 <15:8>								–	3
		0x1E	Frequency Tuning Word No. 3 <23:16>								–	3
		0x1F	Frequency Tuning Word No. 3 <31:24>								–	3
Phase Offset Word 3 (POW3)	0x0A	0x20	Phase Offset Word No. 3 <7:0>								–	3
		0x21	Not Used	Not Used	Phase Offset Word No. 3 <13:8>						–	3
Reserved	0x0B	0x22	Reserved, Do Not Write, Leave at 0xFF								0xFF	N/A
		0x23	Reserved, Do Not Write, Leave at 0xFF								0xFF	N/A

CFR<19>: Clear Phase Accumulator Bit

When CFR<19> = 1, the phase accumulator is synchronously cleared and is held clear until CFR<19> is returned to a Logic 0 state (default).

CFR<18>: Not Used.

CFR<17>: PLL Fast-Lock Enable Bit

When CFR<17> = 0 (default), the PLL's fast-lock algorithm is disabled.

When CFR<17> = 1, the PLL's fast-lock algorithm is active.

CFR<16>

This bit allows the user to control whether or not the PLL's fast-locking algorithm uses the tuning word value to determine whether or not to enter fast-locking mode.

When CFR<16> = 0 (default), the PLL's fast-locking algorithm considers the relationship between the programmed frequency tuning word and the instantaneous frequency as part of the locking process.

When CFR<16> = 1, the PLL's fast-locking algorithm does not use the frequency tuning word as part of the locking process.

CFR<15>: Frequency Sweep Enable Bit

When CFR<15> = 0 (default), the device is in the single-tone mode.

When CFR<15> = 1, the device is in the frequency-sweep mode.

CFR<14>: Sine/Cosine Select Bit

When CFR<14> = 0 (default), the angle-to-amplitude conversion logic employs a cosine function.

When CFR<14> = 1, the angle-to-amplitude conversion logic employs a sine function.

CFR<13>: Charge Pump Current Offset Bit

When CFR<13> = 0 (default), the charge pump operates with normal current settings.

When CFR<13> = 1, the charge pump operates with offset current settings (see charge pump description).

CFR<12:11>: Phase Detector Reference Input Frequency Divider Ratio

These bits set the phase detector divide value per Table 10.

Table 10.

CFR<12:11>	Phase Detector Divider Ratio (N)	Notes
00b	1	Default Value
01b	2	
1xb	4	LSB Ignored

CFR<10>: Charge Pump Polarity Select Bit

When CFR<10> = 0 (default), the charge pump is set up for operation with a ground-referenced VCO. In this mode, the charge pump sources current when the frequency at PD_{IN} is *less* than the frequency at DIV_{IN}. It sinks current when the opposite is true.

When CFR<10> = 1, the charge pump is set up for a supply-referenced VCO. In this mode, the charge pump's source/sink operation is opposite that for a ground-referenced VCO.

CFR<9:8>: Phase Detector Feedback Input Frequency Divider Ratio

These bits set the phase detector divide value per Table 11.

Table 11.

CFR<9:8>	Phase Detector Divider Ratio (M)	Notes
00b	1	Default value
01b	2	
1xb	4	LSB ignored

CFR<7>: Not Used

CFR<6>: Disable Bit for the 2 GHz REFCLK Divider

When CFR<6> = 0 (default), the REFCLK divide-by-2 function is not bypassed. REFCLK input can be up to 2 GHz.

When CFR<6> = 1, the REFCLK divide-by-2 function is disabled. REFCLK input must be no more than 1 GHz.

CFR<5>: SYNCLK Disable Bit

When CFR<5> = 0 (default), the SYNCLK pin is active.

When CFR<5> = 1, the SYNCLK pin assumes a static Logic 0 state (disabled). In this state, the pin drive logic is shut down to keep noise generated by the digital circuitry at a minimum. However, the synchronization circuitry remains active (internally) to maintain normal device timing.

CFR<4:2>: Power-Down Bits

Active high (Logic 1) powers down the respective function. Writing a Logic 1 to all three bits causes the device to enter full-sleep mode.

CFR<4> is used to shut down the analog mixer stage (default = 1).

Phase Offset Control

A 14-bit phase offset (θ) may be added to the output of the phase accumulator by means of the phase offset words stored in the memory registers. This feature provides the user with three different methods of phase control.

The first method is a static phase adjustment, where a fixed phase offset is loaded into the appropriate phase-offset register and left unchanged. The result is that the output signal is offset by a constant angle relative to the nominal signal. This allows the user to phase align the DDS output with an external signal, if necessary.

The second method of phase control is where the user regularly updates the appropriate phase-offset register via the I/O port. By properly modifying the phase offset as a function of time, the user can implement a phase modulated output signal. The rate at which phase modulation can be performed is limited by both the speed of the I/O port and the frequency of SYSCLK.

The third method of phase control involves the profile registers, in which the user loads up to four different phase-offset values into the appropriate profiles. The user can then select among the four preloaded phase-offset values via the AD9858 profile select pins. Thus, the phase changes are accomplished by driving the hardware pins rather than writing to the I/O port, thereby avoiding the speed limitation imposed by the I/O port. However, this method is restricted to only four phase-offset values (one phase-offset value per profile). Each profile has an associated frequency and phase value. Changing the current profile updates both parameters, so care must be taken to ensure that no unwanted parameter changes take place.

Note that the phase-offset value is routed through a unit delay (z^{-1}) block. This is done to ensure that updates of the phase-offset values exhibit the same amount of latency as updates of the frequency tuning word. Otherwise, if the user decides to update both frequency and phase-offset values, the phase-offset change would propagate through the device before the tuning word change. The presence of the unit delay in the phase-offset path ensures that both frequency and phase-offset changes exhibit similar latency.

Profile Selection

A profile consists of a specific group of memory registers (see Table 6). In the AD9858 each profile contains a 32-bit frequency tuning word and a 14-bit phase-offset word. Each profile is selectable via two external profile select pins (PS0 and PS1) as defined in Table 12. The specific mapping of registers to profiles is detailed in the Register Bit Descriptions section. The user should be aware that selection of a profile is internally synchronized with DDS CLK using the SYNCLK timing. That is, SYNCLK is used to synchronize the assertion of the profile select pins (PS0, PS1). Therefore, the PS0 and PS1 pins must be set up and held around the rising edge of SYNCLK. The PS0 and PS1 inputs are designed for zero hold time and 3.5 ns setup time.

Table 12.

PS1	PS0	Profile
0	0	0
0	1	1
1	0	2
1	1	3

The profiles are available to the user to provide rapid changing of device parameters via external hardware, which alleviates the speed limitations imposed by the I/O port. For example, the user might preprogram the four phase offset registers with values that correspond to phase increments of 90°. By controlling the PS0 and PS1 pins, the user can implement π/2 phase modulation. The data modulation rate would be much higher than that possible by repeatedly reloading a single phase-offset register via the I/O port.

AD9858 APPLICATION SUGGESTIONS

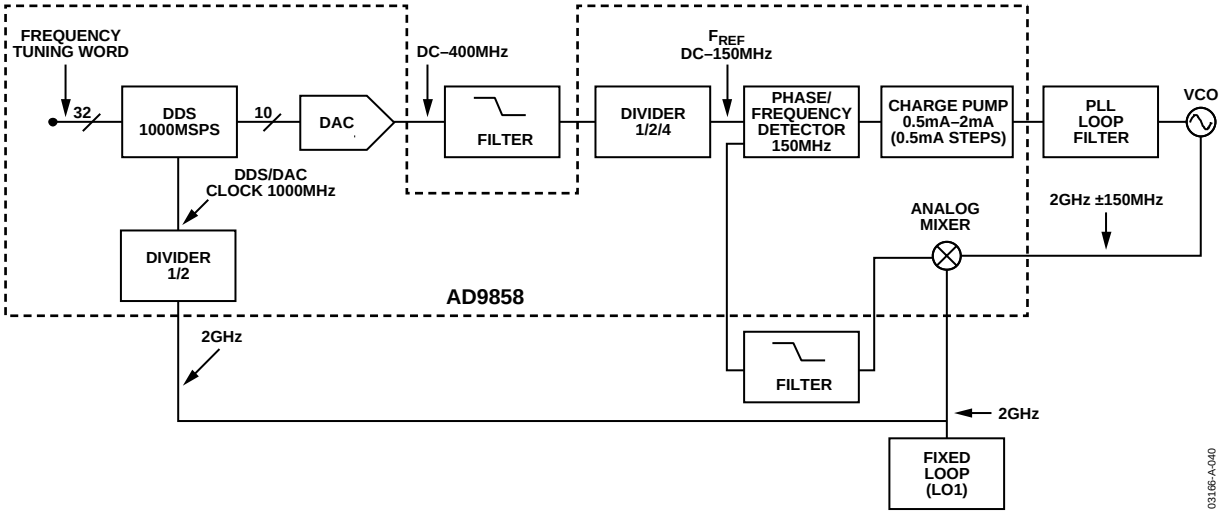


Figure 37. DDS Synthesizer Translation Loop Oscillator (Implemented in Translation Loop Evaluation Board)

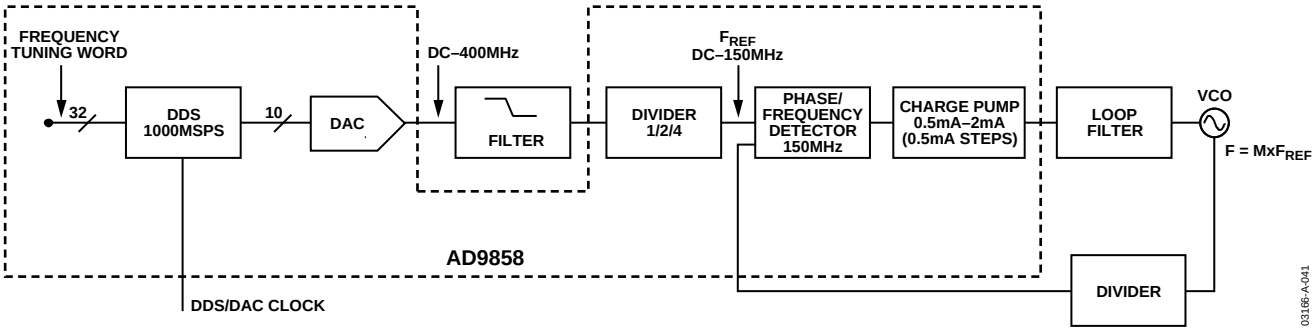


Figure 38. DDS Synthesizer Single-Loop PLL Up-Conversion

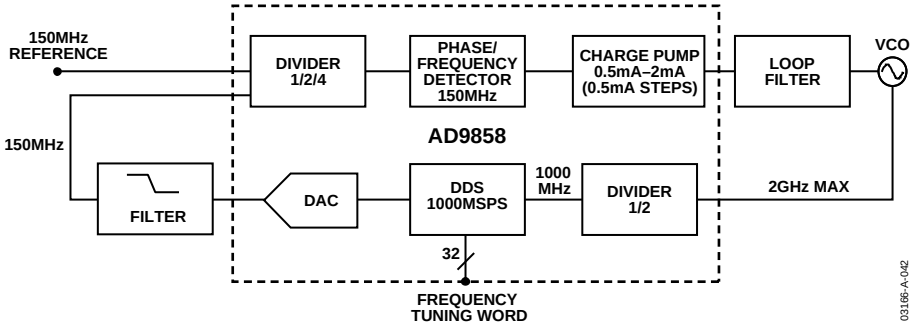


Figure 39. DDS Synthesizer AD9858 as Fractional N Synthesizer (Implemented in Fractional Divide Evaluation Board)

EVALUATION BOARDS

The AD9858 has three different evaluation board designs. The first design is the traditional DDS evaluation board. In this design, the DDS is clocked and the output is taken directly from the DAC. The analog mixer and PLL blocks are made available for separate evaluation.

The second design is a fractional-divide loop. This evaluation board was designed to incorporate the DDS, the phase-detector, and the charge pump. In this application, the DDS is used in a PLL loop. Unlike a fixed divider used in traditional PLL loops, the output signal is divided and fed back to the phase detector by the DDS. To do this, the output signal of the PLL loop is fed to the DDS as REFCLK. The DDS is programmed to match the reference input frequency. Because the DDS output frequency can take on 2^{32} potential values between 0 Hz and one half of the PLL loop output frequency, this enables frequency resolution on the order of 470 MHz, assuming a PLL loop output frequency of 2 GHz.

The third design is a translation loop or offset loop. In this design, the RF mixer is incorporated into the feedback path of the loop. This allows direct up-conversion to the transmission frequency.

The three evaluation boards have separate schematics, BOMS, and instructions. See www.analog.com/dds for more information.

Table 13.

Part Number	Description
AD9858PCB	AD9858 Frequency Synthesizer Board
AD9858FDPCB	AD9858 Fractional-Divide Loop Frequency Synthesizer Board
AD9858TLPCB	AD9858 Translation Loop Frequency Synthesizer Board

OUTLINE DIMENSIONS

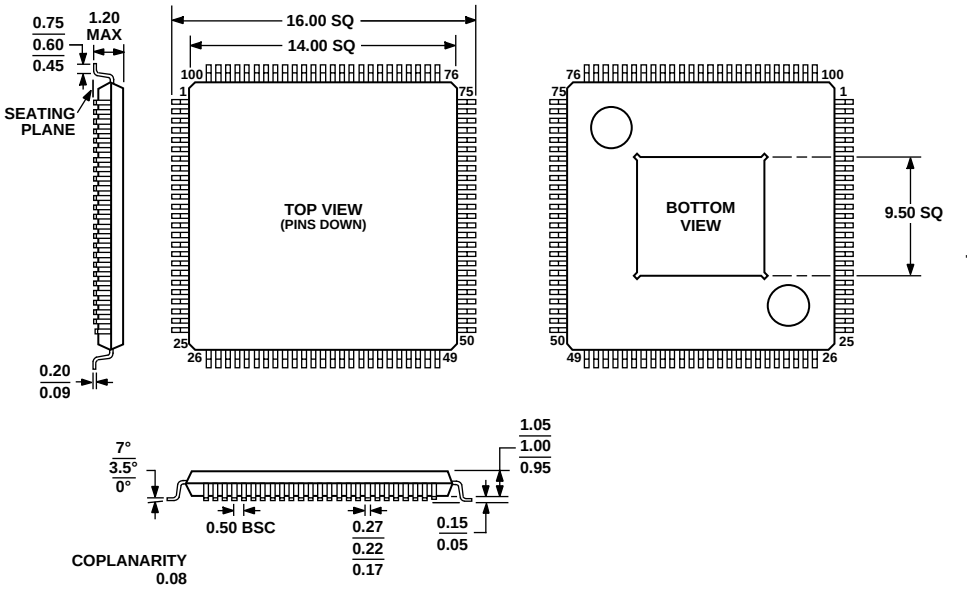


Figure 40. 100-Lead Thin Plastic Quad Flat Package, Exposed Pad [TQFP/EP]
(SV-100)
Dimensions shown in millimeters

WARNING

EPAD (thermal slug) must be attached to ground plane for some other large metal mass for thermal transfer. Failure to do so may cause excessive die temperature rise and damage to the device.

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option
AD9858BSV	–40°C to +85°C	100-Lead EPAD	SV-100
AD9858PCB	25°C	Generic Evaluation Board	
AD9858FDPCB	25°C	Fractional-Divide Evaluation Board	
AD9858TLPCB	25°C	Translation Loop Evaluation Board	

NOTES

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